Design of the Controlled Buck Converter for Wearable Electronic Devices

Tihomir Brusev[1], Georgi Kunov[2], Elissaveta Gadjeva[3]
[1, 2, 3]Technical University of Sofia
Kl. Ohridski 8, 1797 Sofia
Bulgaria
{brusev@ecad.tu-sofia.bg, gkunov@tu-sofia.bg, egadjeva@tu-sofia.bg}

ABSTRACT: *In the current work, we have formulated a controlled buck convertor based on integrated Pulse-Width Modulation (PWM) and Pulse-Frequency Modulation (PFM). This is developed for wearable electronic devices. The input voltage is equal to 3.6V and the average value of the output voltage is regulated to be 1.7V. The maximum efficiency h of the buck converter is 81.43%, when the load current I_{Load} is equal to 68mA. When I_{Load} is smaller than 8mA the efficiency of the PFM controlled buck converter is around 7% higher compared to the efficiency of the PWM controlled buck converter.*

Keywords: Buck converters, Pulse-Width Modulation (PWM), Pulse-Frequency Modulation (PFM), Integrated Circuits, Cadence

Received: 30 May 2020, Revised 29 July 2020, Accepted 9 August 2020

DOI: 10.6025/jes/2020/10/4/138-146

1. Introduction

Today, the number of wearable electronic devices incorporated in the Internet of Things (IoT) systems is growing very fast.

Most of them are battery powered or they use energy from harvesting power sources [1], [2]. Long battery life is required for many portable applications [3]. High efficient buck dc-dc converter integrated together with wearable electronic devices is necessary to be designed and implemented [4]. The block diagram of power management integrated circuit (PMIC) of IoT wearable device is shown in Figure 1 [5]. The input voltage of the buck converter is equal to 3.6V, while the average output voltage is controlled to be equal to 1.7V [5]. On the other hand the output voltage of switching-mode converter is supply voltage for low drop regulators (LDO), which are shown in Figure 1. The monolithic buck converter is necessary to occupy small silicon area and respectively to have small external filter inductor and capacitor components [6].

The PWM controlled integrated buck converter designed on CMOS 0.35 μm technology for IoT wearable device is presented in Section 2. PFM control of the switching-mode regulator is proposed and presented in Section 3. The efficiency η of the designed circuits, when both control techniques are used, is investigated as a function of the load current I_{Load}. The received results are compared and analyzed.

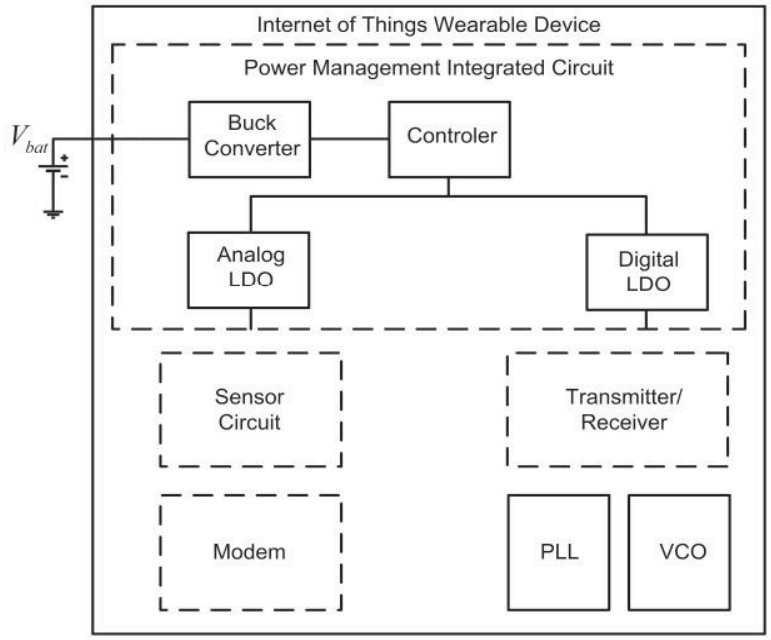

Figure 1. Block diagram of power management integrated circuit (PMIC) in IoT wearable device [5]

2. PWM Controlled Buck Converter

The PWM controlled buck converter is designed for IoT wearable device with Cadence on CMOS 0.35 μm technology. The block circuit diagram is shown in Figure 2.

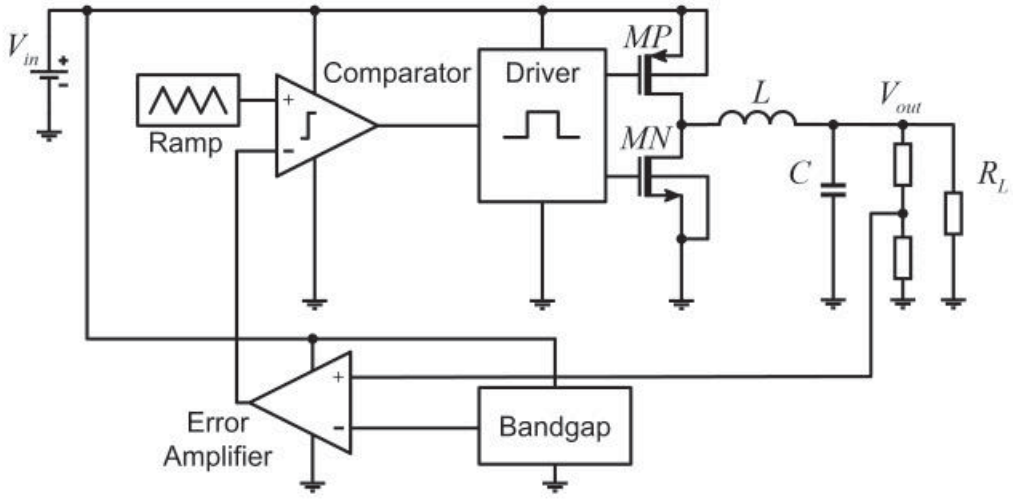

Figure 2. Block diagram of PWM controlled buck converter

The input voltage of the switching-mode regulator is equal to 3.6V and the average value of the output voltage is controlled to be equal to 1.7V [5]. The control system includes bandgap voltage reference, error amplifier, ramp generator and driver. The signal, which regulates the states of buck converter's power MOS transistors, is generated by comparing the voltage with repetitive waveform and error control voltage. The error signal is obtained, when difference between the actual output voltage of the whole system V_{out} and the output voltage level of bandgap reference is amplified. The frequency of the ramp generator

defines the switching frequency f_s of buck converter. This frequency is constant for PWM control technique. The output signal of comparator controls the states of power buck converter's switches. The schematic of ramp generator is presented in Figure 3.

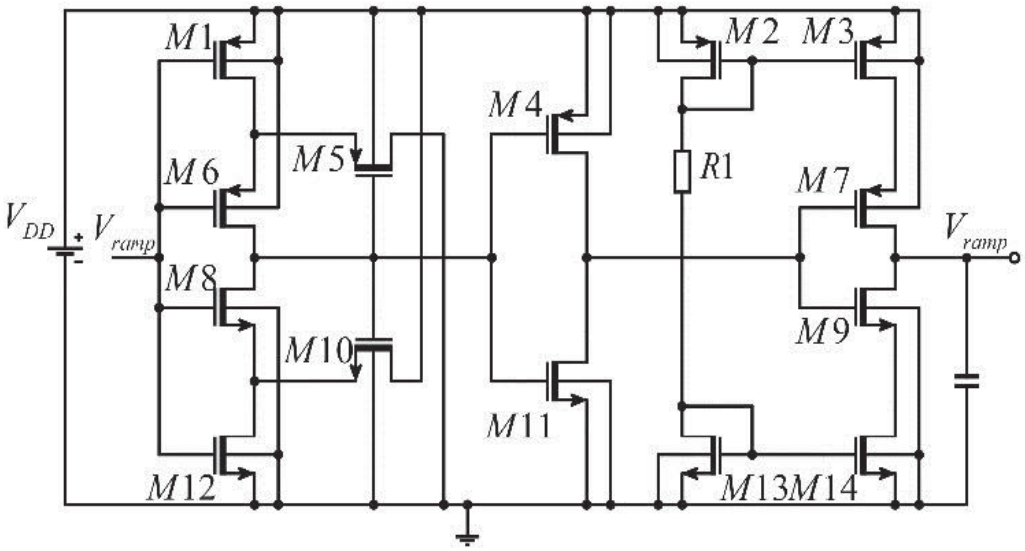

Figure 3. Ramp generator

The output stage of the ramp generator consists of two current mirrors. They define the charging and discharging current of the output capacitor *C1*. The switching frequency f_s of the buck converter depends on the ramp capacitor's value and the current which flows through this component. The waveforms of the output signals of error amplifier, ramp generator and comparator are presented in Figure 4.

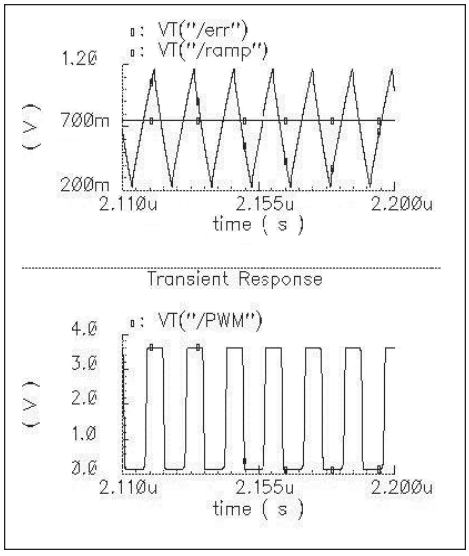

Figure 4. The waveforms of the output signals of error amplifier, ramp generator and comparator

The switching frequency f_s of the designed PWM controlled buck converter is equal to 80MHz.

The waveform of output voltage V_{out} of the designed PWM controlled buck converter is shown in Figure 5. The values of the filter inductor *L* and capacitor *C*, which are used in the lowpass filter, are equal to 250nH and 5nF respectively. The efficiency

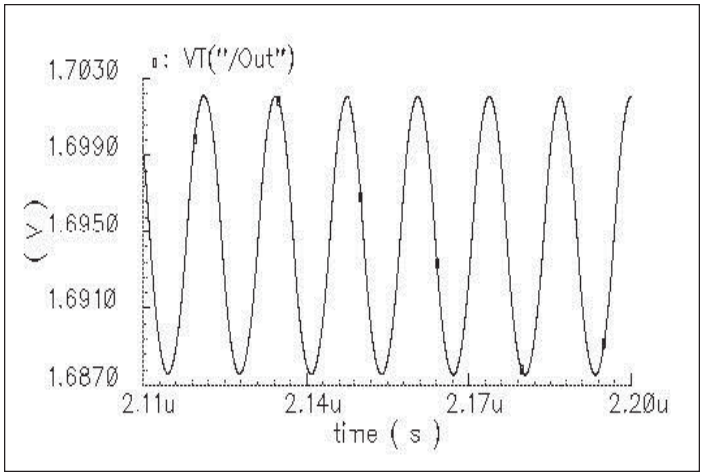

Figure 5. The waveform of output voltage V_{out} of the designed PWM controlled buck converter

η of the buck converter as a function of the load current I_{Load} is investigated. The simulated results are presented in Table 1.

PWM Controlled Buck Converter	
ILoad [mA]	**Efficiency [%]**
100	75.6
80	80.64
68	81.43
50	80.81
30	79.07
20	74.69
10	62.04
8	56.9
5	45.7
2	28
1	17

Table 1. PWM Control Efficiency of Buck Converter as a Function of I_{load}

The efficiency of the switching-mode regulator is calculated by formula:

$$\eta = \frac{P_{out}}{P_{in}} \qquad (1)$$

where P_{out} is the average output power and P_{in} is the average input power of the circuit. The maximum efficiency of the PWM controlled buck converter is equal to 81.43%, when the load current is equal to 68mA. As it can be seen from the received results presented in Table 1, the efficiency of PWM controlled buck converter is decreasing at light loads.

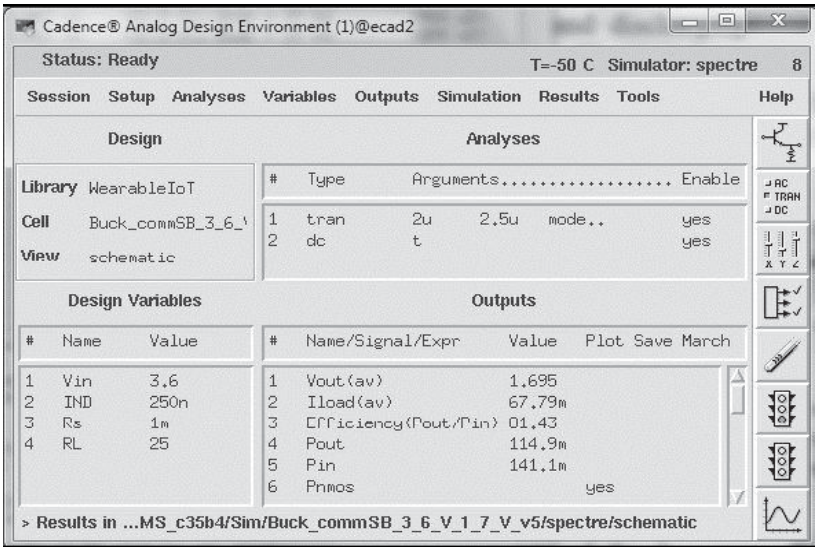

Figure 6. Simulation results received in Cadence Virtuoso Analog Design Environment when I_{Load}=68mA

The simulation results obtained in Cadence Virtuoso Analog Design Environment tool, when the investigated circuit indicates the highest efficiency result, are presented in Figure 6 [7]. The output power of the converter in this particular case is equal to 115mW.

3. PFM Controlled Buck Converter

The PFM controlled buck converter is designed with Cadence on CMOS 0.35 *μm* technology and the block diagram of the whole system is shown in Figure 7. The input voltage of the buck converter is equal to 3.6V, while the output voltage is equal to 1.7V. The control system includes bandgap voltage reference, comparator with hysteresis, oscillator and driver stages. The power MOS transistors are regulated by oscillator with fixed 50% duty-cycle. When the actual output voltage of buck converter is higher than the desired level the control system works in sleep mode. In this case the load energy is delivered by filter capacitor *C*. The only stages which operate at sleep mode of the converter are bandgap and comparator with hysteresis. When the buck converter works in sleep mode of operation driver, oscillator and the power stage are disabled. Thus power losses in control system are minimized in light load conditions.

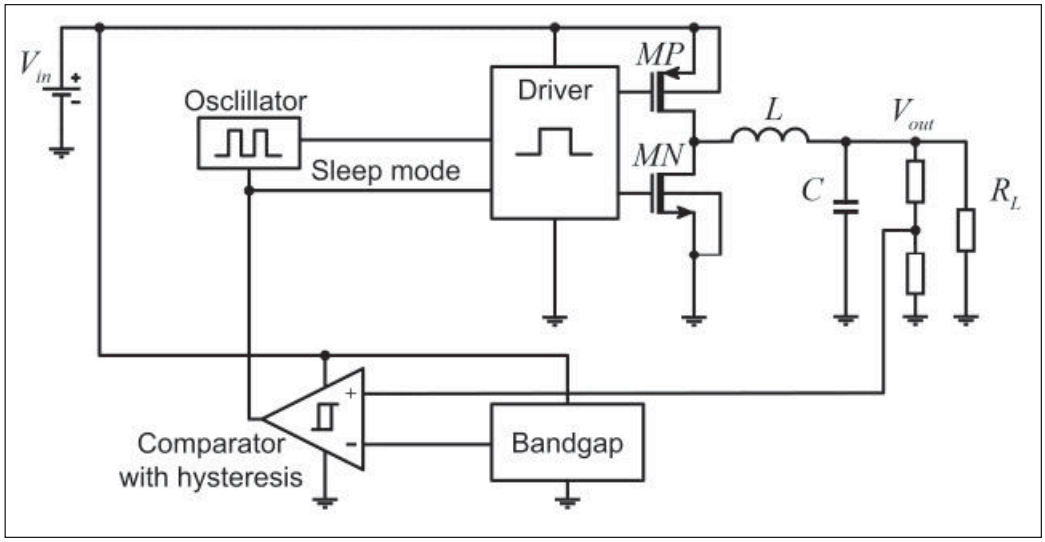

Figure 7. Block diagram of PFM controlled buck

The same bandgap voltage reference is used in this control as in the PWM controlled buck converter. If the output voltage V_{out} becomes smaller than the certain level, the comparator with hysteresis wakes up the whole system. This is the normal mode of operation of the switching-mode regulator. In the pictures bellow the operation of PFM controlled buck converter is presented at different load conditions.

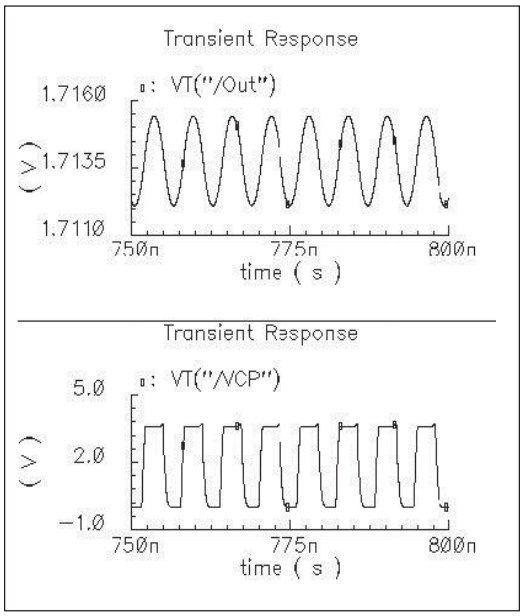

Figure 8. The waveforms of V_{out} and control pulses of main power PMOS transistor V_{cp} when I_{Load} = 8 mA

The waveforms of output voltage V_{out} and control pulses of main power PMOS transistor V_{cp}, when the load current I_{Load} is equal to 8mA, are presented in Figure 8.

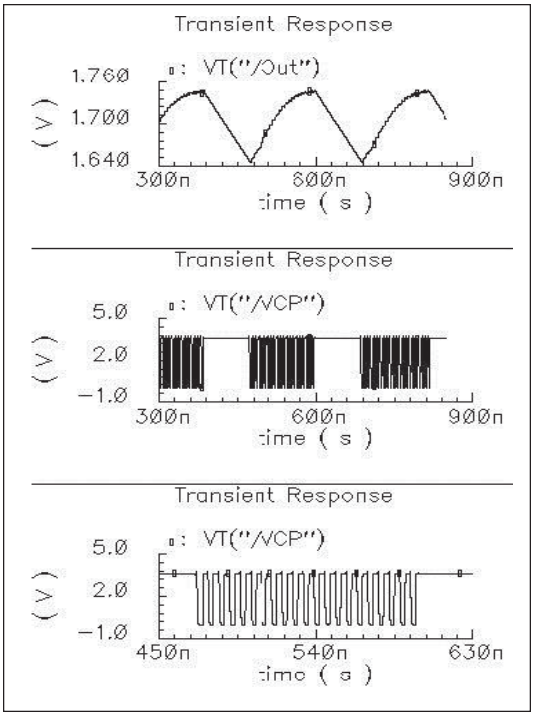

Figure 9. The waveforms of V_{out} and V_{cp} when I_{Load} = 5 mA

The waveforms of the output voltage V_{out} and control pulses of main power PMOS transistor, when the load current I_{Load} is equal to 5mA, are presented in Figure 9. As it can be seen from the pictures shown in Figure 8 and Figure 9 the designed PFM controlled buck converter works in proper manner and the average value of the output voltage V_{out} is equal to 1.7V. The waveforms shown in Figure 9 prove that at light load the system operates longer in sleep mode.

For the oscillator with fixed 50% duty-cycle is used ring oscillator. The schematic of this ring oscillator is shown in Figure 10.

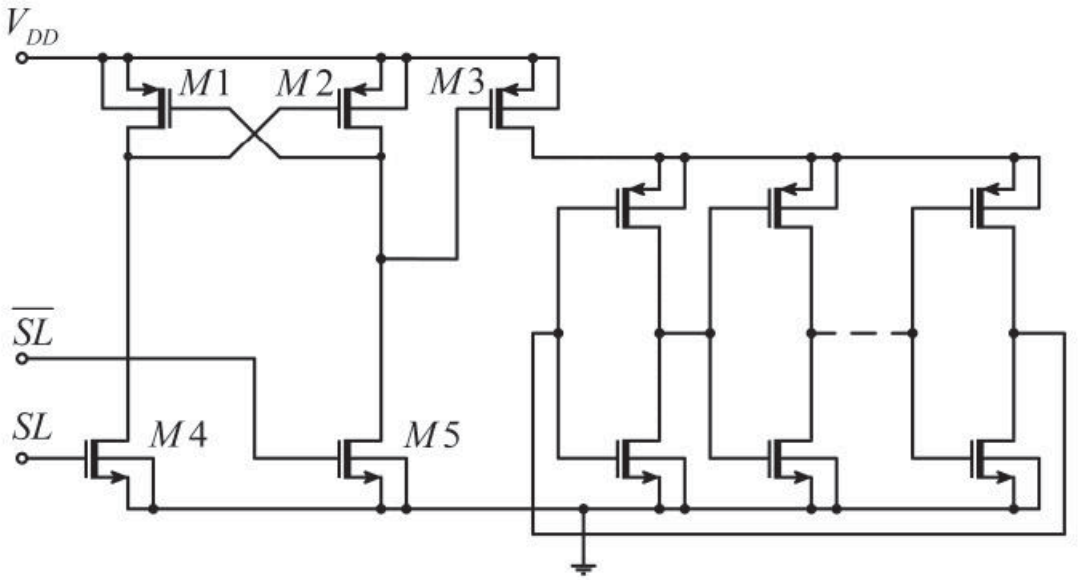

Figure 10. Ring oscillator

The power supply of this stage is switched-off in sleep mode in order to minimize the power losses in the PFM control system. Thus the overall efficiency of buck converter could be increased. If the output voltage of the buck converter V_{out} is higher than the desired voltage, the control signal "*SL"* has high voltage level, while " $\overline{SL}$ " has low voltage level. In this case the transistor *M3*, which is illustrated in Figure 10, is switched off. If V_{out} is smaller than the desired voltage, the control signal " $\overline{SL}$ " has high voltage level and *M3* is switched-on.

The efficiency η results of the PFM controlled buck converter as a function of the load current I_{Load} are presented in Table 2.

PFM Controlled Buck Converter	
I_{Load} **[mA]**	**Efficiency [%]**
30	58
20	60
10	55
8	57
5	54.5
2	35
1	24

Table 2. PFM Control Efficiency of Buck Converter as a Function of I_{Load}

The efficiency results of PWM and PFM buck converter as a function of the load current I_{Load} are graphically presented in Figure 11.

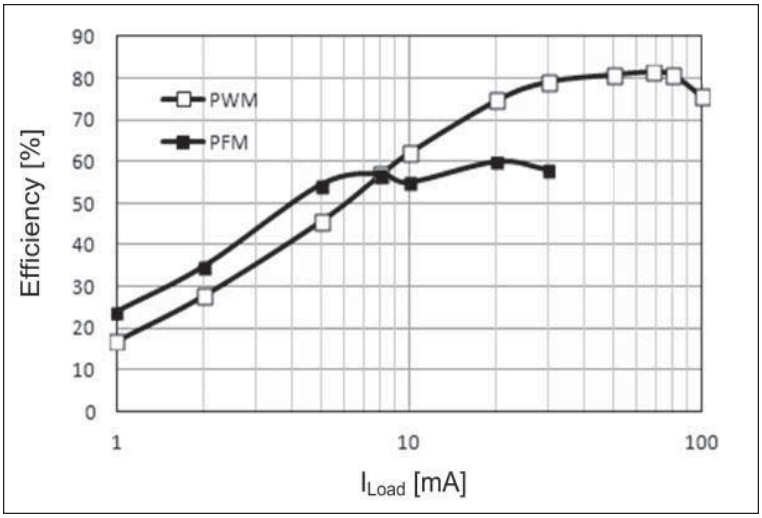

Figure 11. Efficiency of PWM and PFM controlled buck converter as a function of I_{Load}

The obtained results, illustrated in Figure 11 and presented in Table 1 and Table 2, show that the efficiency of the designed switching-mode regulator is higher at light loads if PFM control is used. If I_{Load} is higher than 8mA the PWM is more efficient control technique. When the load current is smaller than 8mA the efficiency of the PFM controlled buck converter is around 7% higher compared to the efficiency of the PWM controlled buck converter. The battery life of wearable electronic devices could be increased if PFM control for switching-mode regulator is used at light loads.

4. Conclusion

Integrated PWM and PFM controlled buck converter designed for low power wearable electronic devices on CMOS 0.35 μm technology has been proposed in this paper. The input voltage is equal to 3.6V and the output voltage is regulated to be equal to 1.7V. The maximum efficiency η of the buck converter is 81.43%, when the load current is equal to 68mA. When the load current I_{Load} is smaller than 8mA, the efficiency of the PFM controlled buck converter is around 7% higher compared to the efficiency of the PWM controlled buck converter. The PFM control technique can increase the battery life of wearable electronic devices used in IoT system, because they operate over a long period of time at light load conditions.

Acknowledgement

This work was supported by the European Regional Development Fund within the Operational Programme “Science and Education for Smart Growth 2014 - 2020” under the Project CoE “National center of mechatronics and clean technologies“ BG05M2OP001-1.001-0008", L2_S1.

References

[1] Cheng, C., Lin, L., Lin, J., Chen, K., Lin, Y., Lin, J. R., Tsai, T. (2017). A DVS-Based Burst Mode with Automatic Entrance Point Control Technique in DC-DC Boost Converter for Wearable Devices and IoT Applications, *2017 IEEE Asian Solid-State Circuits Conference (A-SSCC), Seoul,* 2017, p 121-124.

[2] Paidimarri, A., Chandrakasan, A. P. (2017). A Wide Dynamic Range Buck Converter With Sub-nW Quiescent Power, *IEEE Journal of Solid-State Circuits,* 52 (12), p 3119-3131, December 2017.

[3] Shafiee, N., Tewari, S., Calhoun, B., Shrivastava, A. (2017). Infrastructure Circuits for Lifetime Improvement of Ultra-Low Power IoT Devices, *IEEE Transactions on Circuits and Systems I: Regular Papers,* 64 (9), p 2598-2610, September 2017.

[4] Roy, A., Klinefelter, A., Yahya, F. B., Chen, X., Gonzalez- Guerrero, L. P., Lukas, C. J., Kamakshi, D. A., Boley, J., Craing,

K., Faisal, M., Oh, S., Roberts, N. E., Shakhsheer, Y., Shrivastava, A., Vasudevan, D. P., Wentzloff, D. D., Calhoun, B. H. (2015). A 6.45 μW Self-Powered SoC with Integrated Energy-Harvesting Power Management and ULP Asymmetric Radios for Portable Biomedical Systems, *IEEE Trans. Biomed. Circuits Syst*., 9(6), p 862-874, December 2015.

[5] Park, Y. J., Park, J. H., Kim, H. J., Ryu, H., Kim, S. Y. (2017). A Design of a 92.4% Efficiency Triple Mode Control DC–DC Buck Converter With Low Power Retention Mode and Adaptive Zero Current Detector for IoT/Wearable Applications, *IEEE Transactions on Power Electronics,* 32 (9), p 6946-6960, September 2017.

[6] Spasova, M., Nikolov, D., Angelov, G., Radonov, R., Hristov, N. (2017). SRAM Design Based on Carbon Nanotube Field Effect Transistor's Model with Modified Parameters, 2017 40th International Spring Seminar on Electronics Technology (ISSE), p 1-4, 2017, Bulgaria.

[7] Virtuoso Analog Design Environment, www.cadence.com.