Ultra Low Voltage Converter Construction Principle

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ABSTRACT: *Conversion of voltage from primary to low power sensor modules is related to the micro-power energy harvesting. We in this paper have described the ultralow voltage converter construction and details about the working principle. The significant issue in the design of such converters is the transformer and the switching transistor(s). We further provided the description of the usage of different types of some transistors and transformers, minimum required voltage levels and later some additional directions for further work are described.*

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1. Introduction

Powering sensors and sensor networks often is assisted by harvesting the required energy. Conversion and condition of this energy is mandatory, most of the times from ultra low voltage to somewhat higher voltage. Step up transformers often work with voltages below 0.5 V and power levels in the milliwatt range. They're usually Meissner/Armstrong self oscillating transformers [1]. Some of these converters have starting voltage of about 10 mV [2]. The voltage and power levels on the secondary (or output) winding strongly affect the type and the properties of the switching element not only in the light of efficiency. They also define the operating point levels for the switch. To ensure startup of the converter a "normally on" device is required. Normally on devices are the junction field effect transistors (JFET) since they conduct current with zero gate voltage. Other problems arise including preservation of the transformer self oscillations, efficiency, output voltage. The conducted research strives to summarize the above mentioned problems and to give solution to each one.

2. Construction of Self-oscillating Converter with JFET Switch

Fundamental role in the construction of ultra low voltage self-oscillating step-up converter plays the switching element. Problems caused by the low voltage include:

• Non-linear working region of the transistor;

• Very small driving currents/voltages (according to the switch type);

• Power loss in the transistor;

The JFET transistor comes as the first option for a switching element in the design of ultra low voltage converters. Their "normally on" state allow current flowing through the primary of the transformer, hence magnetizing currents and induced voltage in the secondary (load) winding. This way an oscillation process can begin allowing the further work of the device. Main drawback of the JFET transistor is the channel resistance which leads to: -

• Low efficiency (the channel resistance of the common (non-specialized) JFETs is in the order of tens of ohms);

• Low efficiency of the transformation caused by DC flow. The primary winding usually has very low ohmic resistance and inductive reactance;

To a certain degree these problems may be solved:

• Using several transistors in parallel;

• Increasing the primary's windings and thus effectively increasing the inductive reactance.

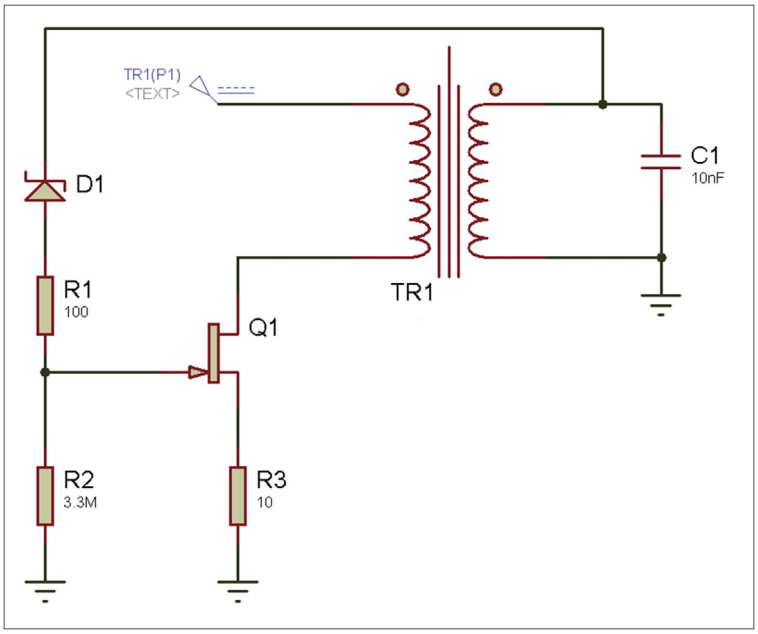

Figure 1. Schematic of self-oscillating step-up transformer

In Figure 1 the basic schematic of self-oscillating transformer is shown. Since the transformer windings are in phase, the current flowing in the primary coil doesn't turn on the transistor (it is "on" with zero gate voltage). The oscillation process started in the LC tank circuit (composed of the secondary winding of the transformer and the C1 capacitor) switches off the transistor Q1 (the network R3, Q1, R1 and D1) in the negative half-cycle allowing a positive feedback.

The diode D1 ensures no forward current flow through the Q1's gate (which would otherwise act as a diode to ground). The resistor R1 limits the gate current flowing back from the gate (remember that despite field driven, the JFET's gate is non-isolated and there is current flow) and may have value of tens of kiloohms. The resistor R2 ties the gate to ground preventing operating point shift.

In Figure 2 the voltage curve at the transistor's drain is shown (channel 1, blue line), as well as the secondary voltage with respect to ground (channel 2, red line). The current drawn by the source can be easily distinguished (channel 1 voltage drop).

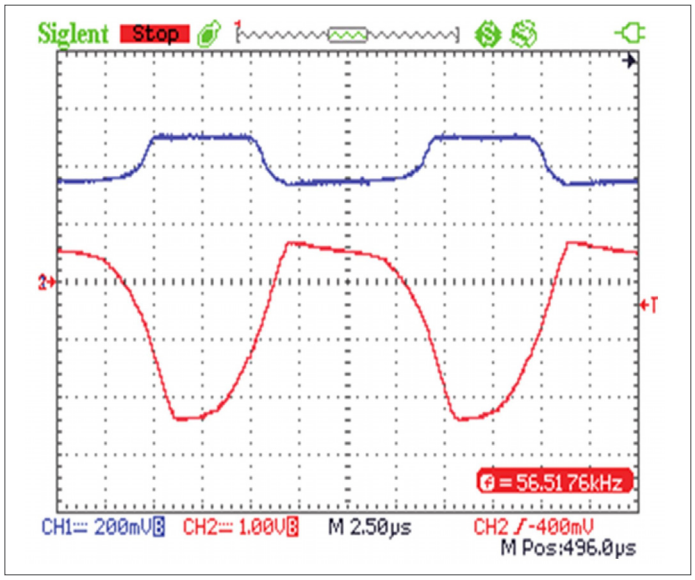

Figure 2. Channel 1 – input voltage (500 *mV*), Channel 2 (red line) – gate voltage

The current flowing through the primary coil is measured across 10 Ω resistor. It can be seen in Figure 3 (channel 1, blue line). Despite the JFET's high channel resistance it is good to ensure short rise and fall times in order to maximize efficiency and to minimize switching losses.

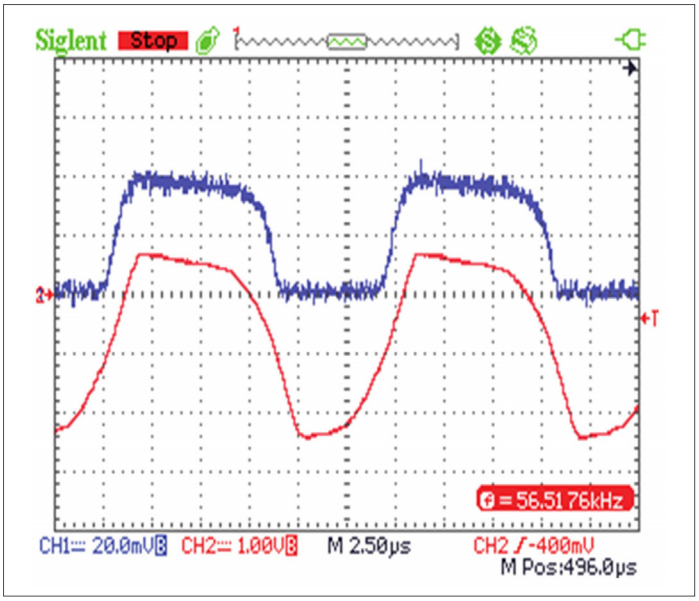

Figure 3. Channel 1 (blue line) is the current measured across 10 Ω resistor. Channel 2 (red curve) is the gate voltage

3. Experiments with Several JFET Transistors in Parallel

For the purpose of the measurements several BF256B transistors were used. The power supply voltage is 150 mV.

The transistor gates are connected according to the schematic in Figure 1. A 10 *k*Ω resistor is put between the diode D1 and each of the gates. The diode D1 is 1N5819 and was found to increase the output voltage (compared to a schematic without the diode).

In Figure 4 the waveform of the output voltage can be seen (channel 1, blue line). The measured peak output voltage for four (4) transistors in parallel is 4 V. The effective supply current is 1.2 *mA*.

The measured values for the peak output voltage versus the number of the parallel transistors are given in Table 3.

Number of transistors	Peak output voltage [V]	Primary current [*mÁ*]
4	4	1.2
3	3	1
2	2.86	0.8
1	0.8	0.8

Table 1. Secondary peak voltage and primary current versus the transistors used in parallel

The increased number of the switches leads to decreased (overall) channel resistance. From Table 3 the current increase can be seen for setups with more transistors.

4. Examination of the Minimum start-up Voltage for Different Types of Transistors

Increased number of transistors was just shown to increase the output voltage. Another key point of the ultra low voltage converters follows to be examined. Important property of the step-up converter is the minimum startup voltage (or the minimum working voltage). In this chapter several types of JFET transistors were used to obtain the lowest working voltage. The results are shown in Table 4.

Transistor	U_{in} [*mV*]	V_{out} *pk* [*mV*]	I_{in} [*mA*]
2SK168	80	500	0.9
BF256B	120	550	0.8
2SK161	50 (120)	400 (1600)	0.4 (0.5)
2SK193	50 (120)	400 (1500)	0.4 (0.55)
2SK192A	70 (120)	500 (2100)	0.7 (0.67)

Table 2. Minimum startup voltage for step up converter without load

The transformer used for the examined minimum startup (input) voltages in table 4 has ratio 3:300, realized with ferrite E cores Kaschke E16/5, material K2006, AL value 1050. For some of the transistors secondary measurement with higher input voltage is given in parenthesis. One may remark the decreased consumption with 2SK192A for higher input voltage. The input current increases slowly together with increasing the input voltage up to about 100 mV. After passing the 100 mV input voltage level the current slowly drops. The effect owes to the better turn off of the transistor. The higher output voltage has greater amplitude (both negative and positive) which leads to fully turned off transistor.

5. Experimenting with Different Transformers

So far the changes and the observation of the schematic concerned the switching element. More information can be acquired with different types of transformers. 3 market available transformers produced by Coilcraft and one custom made transformer were tested. The properties of the transformers are shown in Table 3.

Part number	Ratio	L primary μH	L1 DCR Ω	L2 DCR Ω	SFR (kHz)
253P	1:20	25	0.2	72	580
123Q	1:50	12.5	0.085	200	360
752S	1:100	7.5	0.085	340	230

Table 3. Characteristics of the transformers

The custom made transformer (10:300 K.) has turns ratio of 10:300, ferrite core Kaschke E16/5, material K2006, AL value 1050 without air gap.

The effective input voltage, load (if any) and the peak output voltage are given in Table 4.

Transformer	Transistor	U_{min} *start*	R_{load} (Ω)	U_{out}*pk* [*mV*]
752S	2SK193 L12	80	-	1200
752S	2SK193 L12	500	10000	220
752S	2SK161 Y406	130	-	1680
752S	2SK161 Y406	680	10000	144
752S	BF256B	230	-	1120
752S	BF256B	2000	10000	108
752S	2SK192A	120	-	720
752S	2SK192A	970	10000	100
123Q	2SK193 L12	90	-	1580
123Q	2SK193 L12	300	10000	116
123Q	2SK161Y406	150	-	2240
123Q	2SK161Y406	500	10000	100
253P	2SK193 L12	180	-	2680
253P	2SK193 L12	300	10000	170
253P	2SK161 Y406	300	-	3400
253P	2SK161 Y406	670	10000	208
10:300	K. 2SK193 L12	60	-	1200
10:300	K. 2SK193 L12	170	10000	120
10:300	K. 2SK161 Y406	90	-	2000
10:300	K. 2SK161 Y406	250	10000	120

Table 4. Input and output voltages for the different transformers

Measurements with BF256B were conducted only for single transformer and it was later rejected because the high required input voltage.

6. Reducing the Channel Resistance using a MOSFET Switch

The reason for combining several switching elements in parallel is the high channel resistance of the JFET transistor. MOSFET transistor could be introduced to the schematic in order to optimize the working parameters such as primary current. The JFET switch should always exists in order to ensure the device startup and possibly further oscillations.

Attention should be paid when choosing the MOSFET. Most of these transistors have high gate voltage (up to few volts for the power transistors). The secondary negative voltage should satisfy the NJFET requirements, also the secondary positive voltage should match the working parameters of the chosen NMOSFET.

In Figure 4 is shown possible test setup including both transistors. R1 is used for current measurements. R3 is output load.

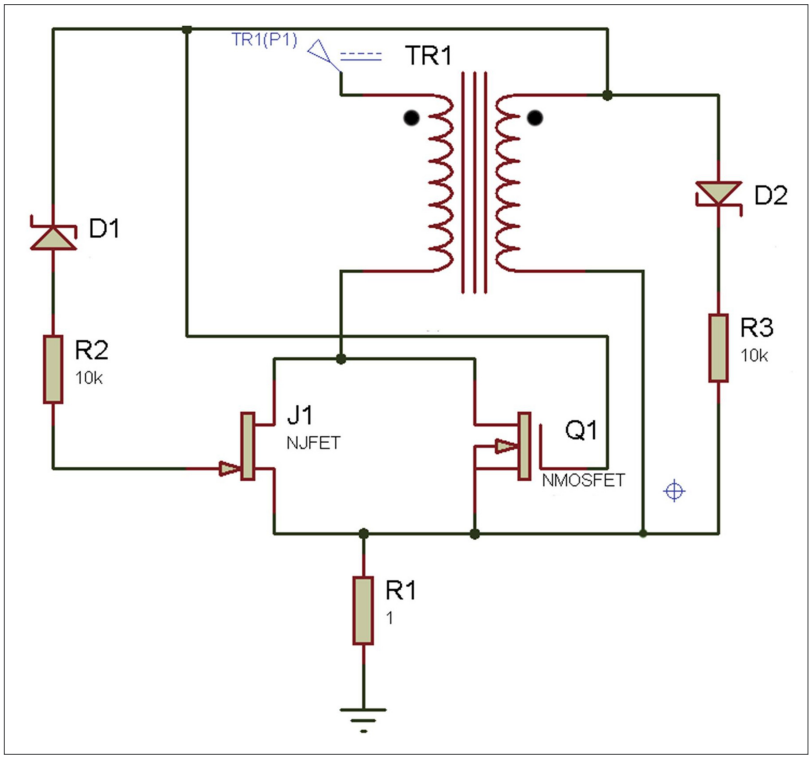

Figure 4. Schematic of self-oscillating transformer with JFET and MOSFET switching transistors in parallel

Two MOSFETs utilizing low gate voltage were found suitable for the schematic shown above. One of them is CETSEMI CEM8208 which drain current versus the gate voltage is shown in Figure 5. It can be seen that voltages above 0.5 V can satisfy the requirements of the ultra low voltage converter (depending on the used transformer).

Another transistor conforming to the above mentioned requirements for low gate voltage is IRLML6344. Its channel resistance versus the gate voltage is shown in table 5.

The MOSFET's gate is directly connected to the secondary coil without any passive element (for reference the NJFET is connected via rectifier). This is to ensure that the MOSFET will conduct current from the lowest possible output voltage. It should be kept in mind that the secondary winding positive and negative voltage shouldn't exceed the maximal gate values as noted in the supplier's datasheet.

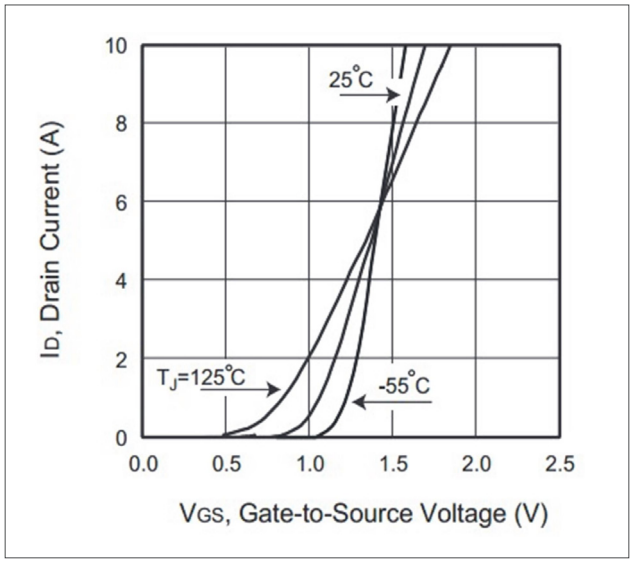

Figure 5. Drain current versus the gate voltage for CETSEMI CEM8208

V_{GS}	R_{DS}	V_{GS}	R_{DS}
0	-	0.7	310k Ω
0.1	-	0.8	~60k Ω
0.2	-	0.9	1.65k Ω
0.3	-	1	171 Ω
0.4	18M Ω	1.1	18.2 Ω
0.5	7.2M Ω	1.2	3.5 Ω
0.6	2M Ω	1.3	<1 Ω

Table 5. IRLML V_{GS} *VS* V_{GS}

7. Further Improvements

The analysis stressed on the use of the switching elements and the transformer. However it can be seen that there is a lot of space for further improvements. Some of them include:

• Utilization of charge pump in order to fully load up the transformer (including both the positive and the negative half cycles).

• Use of synchronous rectifier to increase efficiency and minimize/exclude the voltage drop in the output stage [3].

• Precise (and efficient) output voltage regulation.

Since these types of generators are often used for trickle charge or to charge a super-capacitor (the energy is stored for long time and consumed in short cycles by whatever device is connected to the output) it could happen so that the storage element is overcharged. This may be solved using shunt regulator. However with a view to overall efficiency best is to shut down the generator while it isn't needed. This may be done with a switch to the input of the generator.

8. Conclusion

The conducted research gives detailed information on:

• The type of the switching transistor;

• The operating conditions of the generator under load;

• The parameters of the converter with different transformers;

• Details on keeping the oscillations; - Input and output voltage.

The low input voltage often forces the working point to the non-linear region of the transistor (see the comments for table 2) which will worsen the working parameters. The schematic was improved in several ways.

First the NJFET switch was selected so as to ensure minimum startup voltage.

Second, the JFET's channel resistance problem is solved involving several transistors working in parallel.

Since the second option doesn't give best results, additional proposition for including a MOSFET switch in parallel with the JFET is made.

Third, different types of transformers were used to reveal an important fact, precisely, the transformer's primary winding in these converters often has very low inductive reactance. Ensuring high primary to secondary ratios will force the engineer to make compromise between the primary's inductance versus the turns ratio. The higher the primary's inductance, the higher the efficiency.

Last but not least, the conducted experiments give information on building cheap, simple and reliable ultra low voltage converter.

The conducted research gives details on the usage of ultra low voltage step up converters for use with low power electronics, sensor modules and etc. It provides useful information on some key moments in the design process.

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