PLL Applications for Frequency Analysis using Laboratory Instruments

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ABSTRACT: *In this paper we have outlined a study of PLL and given the laboratory kit. We can deploy it for PLL applications for frequency analysis. Also, we found potential for using it for wireless communication. We suggested the benefits of using laboratory kit and conducted experiments.*

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1. Introduction

Phase-locked loops (PLLs) are widely employed in telecommunications, computers and other electronic equipment. They can be used for frequency synthesis, demodulation, clock recovery, distribution of precisely timed clock pulses in digital circuits, etc. [1]. Frequency synthesizers are indispensable in modern radio communications. Presently, the type of frequency synthesizers most used is based on PLLs [2]. Therefore, the good understanding of PLLs is an important educational aim in the education in electrical and telecommunication engineering.

Currently, computer simulations tend to replace the studying of physically realized devices. Although giving practically unlimited opportunities for studying, computer simulation inevitably leads to some degree of abstraction. This can have adverse effects on the understanding of the studied object and the students' motivation. Pedagogical experience shows that sometimes educators overlook the fact that students' abstract reasoning is not developed to the level, typical for a researcher. The result is mechanically performed actions without understanding their purpose and the practical significance of the results obtained. Without renouncing computer simulations in any respect, we reckon that the use of physically realized laboratory kits is not outdated and can be a valuable part of engineering education.

An example of a popular ready-made laboratory kit allowing the studying of PLLs (in addition to many other topics) is Analog System Lab Kit PRO from Texas Instruments [3]. Unfortunately, its capabilities for studying PLLs are too limited and the helpfulness of using it is questionable.

Many universities use their own laboratory kits or the students themselves build PLLs on breadboards, using popular PLL ICs,

usually CD4046, as in [4]. Such laboratory kits typically have limited capabilities for experiments and are mainly oriented to low-frequency applications, whereas nowadays radiofrequency synthesis tends to be among the most important PLL applications.

Our goal was to develop a laboratory kit for an in-depth study of PLLs with a focus on their application in (but not limited to) frequency synthesis for radio communications. The ability for performing wide range of instructive experiments without needing expensive laboratory equipment was also among the primary considerations. The proposed laboratory kit has been implemented and used in the Department of Radio Communications an Video Technologies in the Technical University of Sofia.

In the next Section, the developed laboratory kit is presented. In Section 3 demonstrations and a laboratory session plan are suggested.

2. Laboratory Kit Description

A Slightly simplified schematic diagram of the laboratory kit is presented in Figure 1.

The core of the PLL is TSA5511, a popular synthesizer IC from NXP Semiconductors. Although it is relatively old, similar ICs are offered for new designs, for example ADF4002 [5] from Analog Devices. A very useful feature of TSA5511 for our purposes is its ability to route the two phasefrequency detector (PFD) inputs to two of the general purpose IC outputs/inputs.

The main loop filter is made up of the built-in amplifier, selectable RC networks for frequency dependent negative feedback and some additional components which are not shown for the sake of clarity. In positions 1 and 2 of switch S4, the recommended filter topology is selected. In position 1, the resistor is variable, whereas in position 2 it is fixed at a nearly optimal value and the capacitances are nearly an order of magnitude smaller than in position 1. In position 3, the minimum number of components that ensure an acceptable stability margin are used. In position 4, the phase margin is nearly zero (but the system is still stable). In positions 1-4, the loop filter acts as an analog memory retaining the steady state control voltage and its gain (theoretically) approaches infinity at DC, whereas in position 5 the loop filter acts as a usual low-pass filter having a finite gain from DC to a certain cutoff frequency. In order to demonstrate an unstable loop, anadditional low-pass filter can be included by setting S2 in the upper position.

The voltage controlled oscillator (VCO) is implemented as an LC oscillator with a pair of varactors for frequency control. The tuning sensitivity can be chosen from two values. It is useful for some experiments to be able to change of the VCO free running frequency (FRF). Typically, in practical implementations, this is performed by adjusting the inductance in the oscillator LC tank. In our case this is not very convenient. For this reason, an auxiliary VCO control input is provided. It allows to change the VCO FRF in a relatively wide range. In addition, it allows to modulate the input is provided. It allows to change the VCO FRF in a relatively wide range. In addition, it allows to modulate the VCO FRF by an laboratory LF generator. This is useful for two purposes: (1) To examine the ability for frequency modulation of the synthesized oscillation and (2) To examine the ability of the PLL to suppress the VCO phase noise components at different offset frequencies. It is known that phase noise measurement is a rather complicated task for the students, which requires special theoretical training and/or expensive equipment [6], [7]. In our case, an intentional sinusoidal modulation of the VCO FRF (and the corresponding phase modulation) can imitate the phase noise components at particular frequency offsets. Since the modulation index can be set at a sufficiently high value, no sensitive equipment or advanced techniques are needed for the measurement. Naturally, the modulation index should not be too large to maintain the linearity.

In order to demonstrate the benefits of using PFDs in PLLs, an auxiliary path is implemented, in which a plain phase detector (PD) is employed. When S1 is in the upper position the PLL uses this path.

The control unit has the following functions: To enable the setting the frequency division ratio *N1* of the programmable counter; to enable the selecting of the charge pump current (TSA5511 offers 50μA and 220 μA); to enable the setting of a second division ratio *N2* and automatically alternate the programmable counter division ratio between *N1* and *N2* in a periodic manner. The last capability of the control unit is useful when the transient behavior of the PLL is examined. In this case, the control voltage is observed by Oscilloscope 2. The periodic repetition of the transients makes it possible to see almost

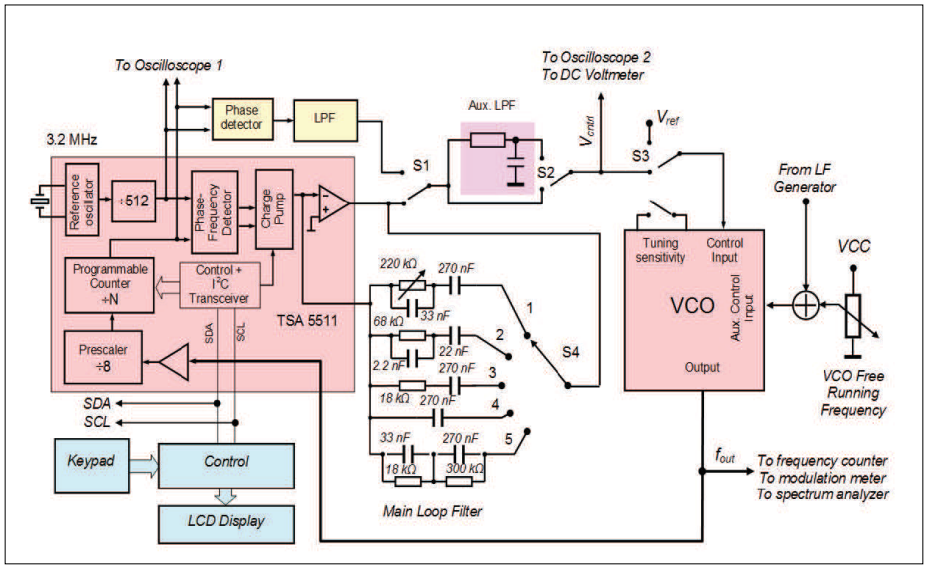

Figure 1. Simplified schematic diagram of the laboratory kit

immediately the results caused by the changes in the loop filter and also enables the use of oscilloscopes without a storage capability.

3. Suggested Laboratory Session Plan and Demonstrations

3.1. Steady State of the PLL

First, the students are asked to compose an equation based on the laboratory kit diagram, in which the synthesized frequency is unknown, and to solve it in order to obtain the relationship between the division ratio N and the synthesized frequency. Based on the result they should also determine the frequency step of the synthesizer.

Next, the laboratory kit is powered up with the switches in the positions depicted in Figure 1. The control unit automatically sets the default frequency division ratio $N1 = 2000$. Then the students are asked to check whether the frequency counter readout agrees with the theoretical prediction.

Further on, the students are asked to look at Oscilloscope 1 and to say if the frequencies of the phase detector inputs are really equal to each other and if it is possible to detect a very small frequency difference (if there is such). Then the teacher can make the following demonstration: He sets S3 in the upper position (so that the automatic frequency control is terminated) and one of the two oscillograms begins to move. After that, he tries to stop it by adjusting the VCO FRF, which fails, making it clear that even the slightest frequency difference can be detected as an oscillogram motion. Then he restores the control loop and the oscillogram freezes. Now it is the proper time to draw the students' attention to the fact that the steady state frequency error in PLLs is zero [8], [1]. This is especially necessary if the students are not trained in control system theory. Often, when learning negative feedback systems in Signal and Systems course, telecommunication students do not consider them in an automatic control perspective. Hence, they do not readily recognize that there is a non-zero steady state error in a typical negative feedback control system and are not impressed by the zero steady state error in the PLLs. Then the teacher can explain that the zero steady state frequency error of PLLs, combined with the impeccable maintaining of the intended frequency division ratios of the digital frequency dividers, makes the output frequency strictly related to the reference oscillator frequency.

Then the students examine the dependency of the output frequency and the control voltage on the VCO FRF with a fixed frequency division ratio N. The FRF is varied approximately from 70 to 130 MHz. In order to measure the VCO FRF, the switch S3 should be set in the upper position. (For the purpose of this laboratory session, "VCO FRF" should be understood as the VCO frequency when the control voltage is equal to a fixed reference value.) The relationships are graphically presented. The students are asked to designate on the graphs the VCO FRF range, corresponding to the inlock condition and to explain

briefly the behavior of the PLL system.

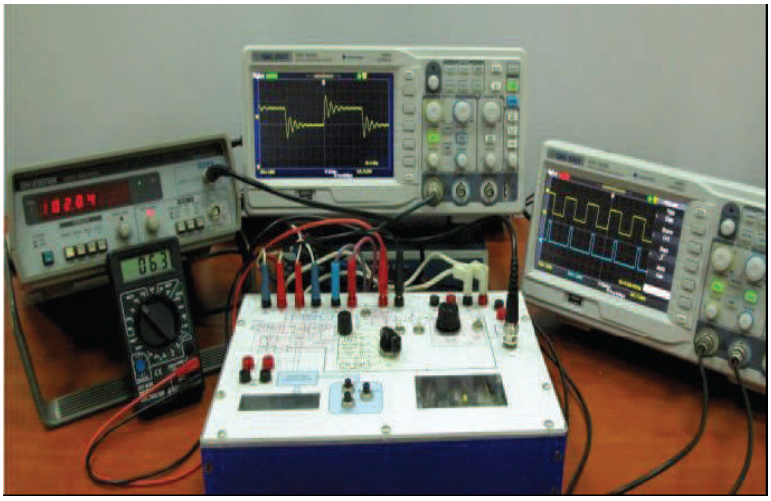

Figure 2. The proposed kit in use (at the moment of taking the photo, the variable resistor in the loop filter is not adjusted to its optimal value

The next task is to determine the synthesized frequency range of the synthesizer, provided that the VCO FRF by design is 100 MHz for example, which under normal operating conditions can change within a certain range, e. g. ±1 MHz. Based on the findings in the previous task, the students should be able to deduce what the worst conditions for the synthesis of the minimum and maximum frequencies are. Then, after setting the corresponding VCO FRFs they should pick out experimentally the minimum and maximum *N* values, for which the in-lock condition is still maintained. For the minimum and maximum synthesized frequencies, the corresponding control voltages should also be written down in the lab record. Then the students should propose ways for modifying (widening/narrowing and translation up/down) the synthesized frequency range of a PLL synthesizer.

Finally, the students should find the synthesized frequency errors for a few frequency division ratios and identify the cause for these errors. It is now the appropriate time to remember that PLLs themselves have zero steady state frequency error, that the digital frequency dividers strictly maintain the intended division ratios and that the output frequency is strictly related to the reference frequency. Basedon these considerations, the students are expected to conclude that the error is caused by the reference frequency inaccuracy.

Steady state phase errors. Although in the context of frequency synthesis, the phase error has little significance, it can be important for other PLL applications. The students can change the frequency division ratio *N* and the VCO FRF and observe the steady state phase error for the five S4 positions on Oscilloscope 1. They can see that the phase error is also zero (besides the zero frequency error) for positions 1-4 [1]. For position 5, there is a nonzero phase error which changes depending on the VCO FRF and the *N* value.

3.2. Dynamical Behavior

The **transient behavior** can be examined first. The teacher should outline the reasons why transient behavior is important, especially if the students are not familiar with the concepts of control theory [8]. It should be emphasized, among other things, that the look of the transient response is informative about the stability margins of the system [1]. Then the control unit should be put in the "Transient" mode and a second frequency division ratio *N2* should be set (for example *N2*=2050 if *N1*=2000). This ensures an automatic alternation of the programmable counter division ratio between *N1* and *N2* in a periodic manner. Then the teacher explains the oscillogram on Oscilloscope 2: What part of the oscillogram corresponds to a steady state, in what moment the *N* value is changed, and (approximately) when the corresponding new frequency settles.

Then the students should examine the PLL transient response for the two charge pump currents with S4 in position 1 when the

resistor value is changed. They should sketch out the transient responses for the optimum and for one markedly inappropriate value of the resistor for each charge pump current setting and write down their durations. Transient responses for positions 2 and 3 should also be examined for each charge pump current setting. Finally, the obtained transient response durations should be compared and conclusions should be drawn and shortly written in the lab record.

Next, the transient response for position 4 should be observed. It should be sketched and its duration should be measured and written down. At this point the students should be able to explain what the function of the loop filter components in positions 1, 2 and 3 from theoretical and from practical point of view is.

A stable vs. an unstable loop. In the next experiment the frequency division ratio is fixed and an additional low-pass filter is included in the loop. It could presumably further reduce the reference spurs in the output oscillation. In reality, the PLL becomes unstable. The students have studied about stability in mathematics, circuit theory and analog electronics. However they are often not aware of the exceptional practical significance of this concept, erroneously thinking that it relates to the consistency of the performance or endurance. Therefore, it is necessary that they observe an unstable system at least once in order to realize that a system is not operational at all if it is not stable. Additionally, it should be explained that PLLs are inherently prone to instability as a result of the accumulated phase lags caused by the integration (which models the VCO behavior with respect to the phase in the linear PLL model [1]) and by the low-pass filter in the loop.

Acquisition. When the phase-frequency detector is used, it greatly facilitates the acquisition, as a result of which the corresponding phenomena cannot be observed. When the plain phase detector is used (S1 in the upper position), the typical beat frequency oscillation in the control voltage can be seen on Oscilloscope 2. Initially, the VCO FRF is changed (up or down) until the PLL unlocks. Then the VCO FRF is slowly changed towards approaching the acquisition range. It can be observed that the beat frequency decreases, the voltage swing increases and finally the PLL locks.

Examining the reference spurs in the VCO oscillation. Although a spectrum analyzer would be useful for this purpose, the reference spurs can be roughly estimated by measuring the reference component in the control voltage. It would be advantageous in this case, if Oscilloscope 2 has a good Y channel sensitivity, e. g. 1 mV per division or even less. With the Y input AC coupled and a sufficiently high Y gain setting, the reference component in the control voltage should be evaluated qualitatively and quantitatively for the 5 positions of S4. Then the reference spur level can be roughly estimated using the VCO sensitivity.

A special attention should be paid to the reference components in position 5, when the loop filter is a usual lowpass filter which no longer retains the steady state control voltage. This case is especially important for understanding the benefits of using a PD output configuration with a charge pump.

Frequency modulation capability examination. In this case an LF sine generator and a modulation meter should be connected according to Fig. 1. The sine magnitude is chosen so as to obtain an output frequency deviation of a few tens of kilohertz when the frequency is of the order of kilohertz. Then the dependency of the frequency deviation on the modulation frequency is examined. Alternatively the control voltage swing can be measured on Oscilloscope 2 if a modulation meter is not available. In this case, it would be advantageous if the modulation signal is also observed on the second Y channel. For sufficiently low modulation frequencies, the loop succeeds to track the VCO frequency variations and produces corresponding control voltage variations which suppress the modulation. When the modulation frequency rises enough, the control voltage swing decreases and the loop no longer counteracts the modulation successfully. This experiment also makes possible the evaluation of the transfer function of the PLL for the VCO phase noise components if some additional calculations are performed.

3.3. PLL Ranges

PLL ranges [1] can be examined by changing the VCO FRF. When the PFD is used, there is no difference between the hold-in and the acquisition range from the observer's point of view: As a result of the sensitivity of the PFD to the frequency differences, the VCO frequency is pulled towards its in-lock value and the acquisition happens readily. When the plain PD is used, the students can observe a fairly large difference between the hold-in range and the acquisition range. Additionally, they can observe in this case an inclination of the PLL to false lock conditions where the frequencies on the PD inputs are related by ratios of small integers.

3.4. Theory vs. Experiment

It would be very instructive in an advanced course if the students compose the linear model of the loop and calculate the building block parameters based on the laboratory kit data. The VCO sensitivity can be easily evaluated experimentally. Then the students can predict the loop behavior theoretically (or by simulations) and compare the predictions with the experimental results.

4. Conclusion

A laboratory kit for an in-depth study of PLLs was designed and implemented. The experience gathered during its use showed that the intended goals were reached. The operating capabilities of the kit satisfy the requirements of the undergraduate curriculum in Telecommunication Engineering and also offers additional opportunities for further studying PLLs for students with special interest in the area of radio communication devices.

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