# Use of Standard Two Phase DC Converter Architecture for ZVS Technique

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***ABSTRACT:*** *The CMOS technology with Cadence is used to generate a two-phase switching mode for the dc converter with zero voltage switching. Further, the main power transistors-based loss is measured. We found that the effectiveness of the system increases marginally when the help of the standard two-phase dc converter architecture where we have deployed the ZVS technique.*

**Keywords:** Two-phase switching-mode Converter, Zero Voltage Switching (ZVS), Efficiency, CMOS Technology, Cadence

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## 1. Introduction

Today smart phones can transfer large data packages in a real time, thanks to the fourth generation Long-Term Evolution (4G LTE) wireless communication standard. The great functionality of modern telecommunication devices is due to the use of OFDM (Orthogonal Frequency-Division Multiplexing) modulation. The signal is transferred by several sub-carrier frequencies, which are summed at the output of modulator. Thus the spectrum in 4G LTE standard is used much more effectively [1].

On the other hand the sizes of the new mobile phones became larger, which allows increasing of the battery dimensions. Nevertheless, the time between two consecutive charges is small. The efforts of the designers are focused over the increasing of power supplies efficiency. Those circuits have to ensure the desire energy of transmitter's power amplifier (PA). The standard switching-mode dc-dc converter cannot fulfill the requirements to deliver appropriate fast dynamically changeable output voltage to drain or collector, respectively of MOS or BJT RF transistor of PA.

The power supply circuit, which provides the desire energy to transmitter's PA is called envelope amplifier. The block diagram of envelope tracking power amplifier's system is shown in Fig. 1. Envelope amplifier delivers the drain or collector supply voltage of PA's transistors [2]. It dynamically changes this supply voltage according to the variations of the PA input signal**.** The envelope amplifier tracks the PA input signal and controls the PA supply voltage according to the envelope of this signal. The efficiency $\eta_{ET\,PA}$ of the envelope tracking power amplifier's system is equal to [3]:

$$\eta_{ET\,PA} = \eta_{ET\,.\,PA} \tag{1}$$

where $\eta_{EA}$ is the efficiency of the envelope amplifier; $\eta_{PA}$ is respectively the efficiency of the PA. The run-time of wireless communication devices could be increased if envelope amplifier with high efficiency is designed.

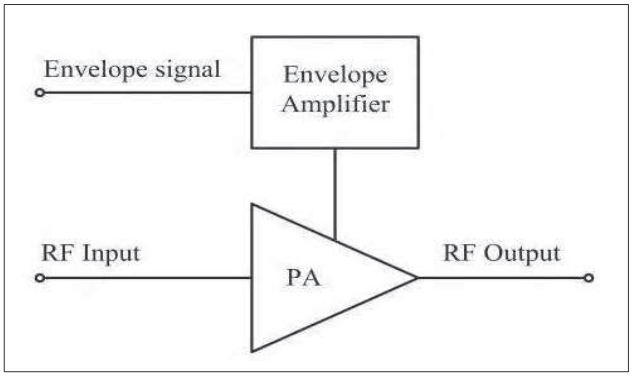


Figure 1. Envelope tracking power amplifier's system

Most of the envelope amplifier's architectures include parallel or series connected linear amplifier and switchingmode dc-dc converter. Switching-mode converter ensures between 70% and 80% energy delivered to PA [2]. Therefore, high efficient dc-dc converter could improve significantly the efficiency of envelope amplifier. One of the features of switching-mode converters is that they are good choice only when relatively low-data rate communication signal is transferred. The tracking speed of the switching-mode converter could be increased if the single phase dc-dc converter is replaced by two-phase converter. Thus the portion of energy distributed from low efficient linear amplifier in envelope amplifier will be smaller, compared to the case when the switching-mode amplifier is a single phase dc-dc converter. This leads to improving of the overall efficiency of envelope tracking power amplifier system.

The tracking speed possibilities of standard synchronous single phase dc-dc converter and two-phase interleaved buck converter are discussed in Section 2 *A* of this paper. In Section 2 *B*, the Zero Voltage Switching (ZVS) technique is considered, which helps to reduce power losses in the main transistor of switching-mode dc-dc converters. Two-phase dcdc converter with ZVS is designed with Cadence on CMOS 0.35 $\mu m$ process. Power losses in the main power MOS transistors are considered and evaluated. The efficiency results of two-phase dc-dc converter with ZVS are evaluated and compared to the efficiencies of the standard two-phase interleaved dc-dc converter. The received results are presented in Section 3.

## 2. Switching-mode Converters

### 2.1. Single phase and Two-phase Switching-mode Converters

The standard synchronous single phase dc-dc converters, shown in Figure 2, indicate high power losses in the inductor at large values of the inductor current ripple $\Delta i_L$. The two-phase converter structure helps to reduce this negative effect [4].

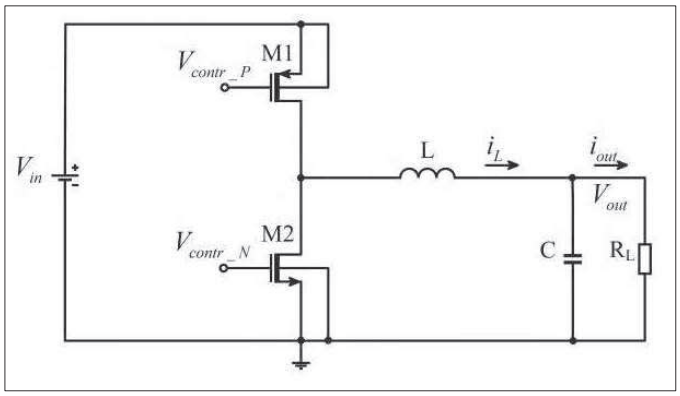


Figure 2. Single phase dc-dc converter

The two-phase interleaved dc-dc converter architecture, presented in Figure 3, leads to reduction of the output current ripple $\Delta i_{out}$ of the circuit. The reason is that the phase sifted inductor current ripples respectively of the first and second sub-converter stage $\Delta i_{L1}$ and $\Delta i_{L2}$ are summed at the output.

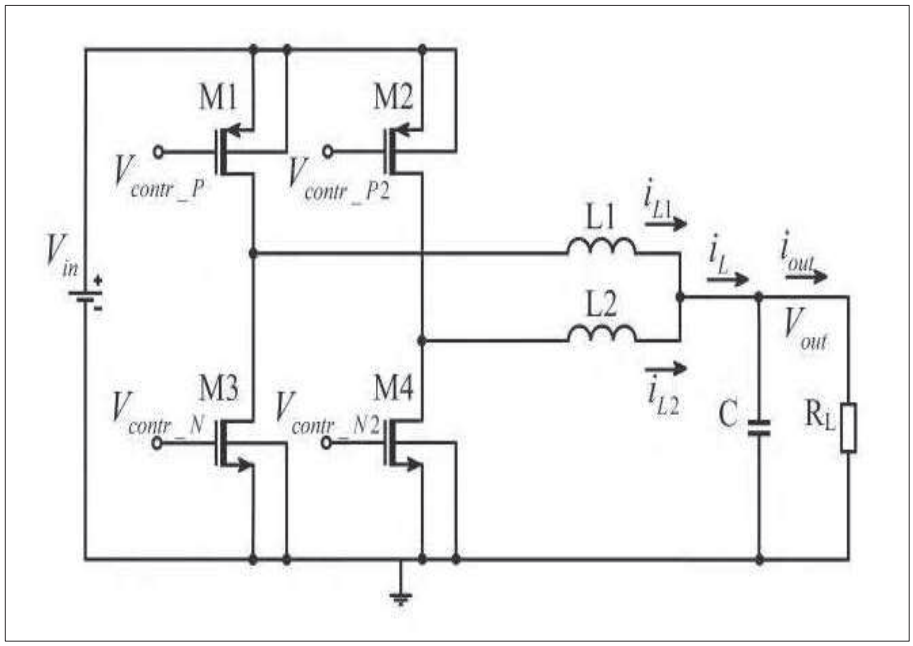


Figure 3. Two-phase interleaved dc-dc converter

The output current ripple $\Delta i_{out}$ of the two-phase interleaved buck converter with non-coupled inductors can be expressed in the form [5]:

$$\Delta i_{out} = \frac{V_{out}}{L}\left(1-2D\right)T_s, \tag{2}$$

where $T_s$ is the switching period of converter, $L$ is the value of filter inductors (if $L1 = L2$, which is the case of the investigated dc-dc converter architecture).

Minimum values of the output current ripple $\Delta i_{out}$ can be Received if the duty cycle of the converter $D$ is close to 0.5. The inductor current ripples $\Delta i_L$ of the single phase buck dc-dc converter and two-phase interleaved buck converter with noncoupled inductors have equal values, and can be expressed in the form [5]:

$$\Delta i_L = \frac{V_{out}}{L}\left(1-D\right)T_s\,. \tag{3}$$

In two-phase interleaved dc-dc converters architectures the same output current ripples as those of single-phase dc-dc converters could be established with smaller values of output filter inductors respectively $L1=L2$. These phenomena could be very useful for LTE applications power supply circuit, when envelope amplifier has to be fast in order to track high frequency envelope signal. The two-phase dc-dc converter could replace the single phase switching-mode regulator in parallel hybrid envelope amplifier structure. Thus most of the energy delivered to power amplifier can be ensured from fast and high efficient switching-mode multiphase dc-dc converter. The portion distributed from low efficient linear amplifier will be smaller, compared to the case when switching-mode amplifier is a single phase dc-dc converter, improving the overall efficiency of envelope tracking power amplifier system.

### 2.2. Zero Voltage Switching

The circuit of synchronous single phase switching-mode buck dc-dc converter with ZVS is shown in Figure 4. The advantage of those types of circuits is that the main power transistor *M1* can be switched-on and switched-off respectively at zero voltage [6].

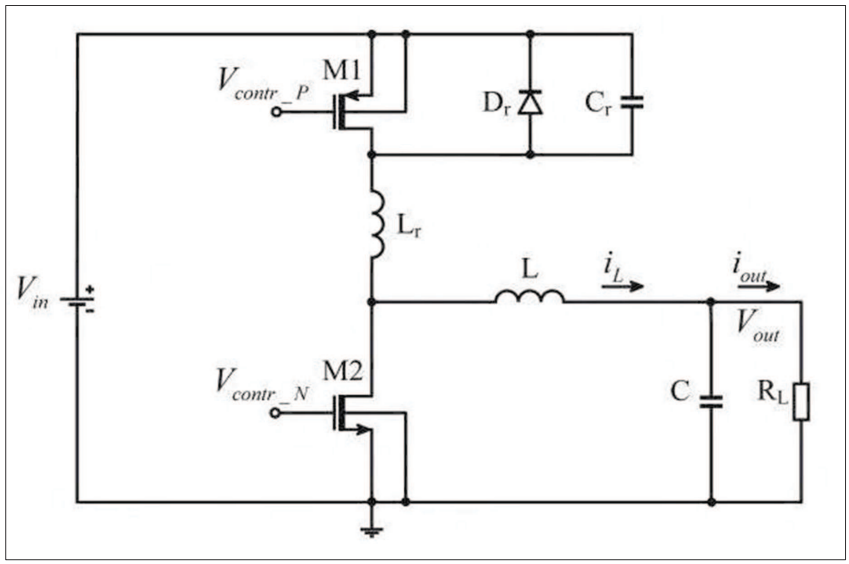


Figure 4. Single phase dc-dc converter with ZVS

The zero voltage switch-off of the main PMOS transistor *M1* of dc-dc converter is because of the capacitor *Cr*. The Zero voltage switching-on state of the PMOS transistor *M1* is ensured by the diode $D_r$. The function of this component is to clamp to zero capacitor voltage $V_c$, when transistor *M1* is at switch-off state [6].

The effect of ZVS will lead to zero switching power losses of main PMOS transistor *M1*. Thus the total power losses in the MOS transistors of synchronous dc-dc converter could be decreased. They are equal to [7]:

$$P_{tot,MOS} = a\sqrt{\left(I^2 + \frac{\Delta i_L^2}{3}\right)} f_s, \tag{3}$$

where $\Delta i_L$ is the inductor current ripple, $I$ is a dc current supplied to the load, and $a$ is a coefficient depending on the equivalent series resistance of the transistors, the input total capacitance of the MOS transistors $C_{tot}$, and the power supply $V_{in}$. The decreasing of total power losses in MOS transistors of dc-dc converter will improve the efficiency of the circuit. The efficiency of the buck dc-dc converter can be expressed by:

$$\eta = \frac{P_{out}}{P_{out} + P_{losses}}, \tag{5}$$

where $P_{out}$ is the output power of the dc-dc converter; $P_{losses}$ are overall power losses in the dc-dc converter.

### 3. Investigation of Two-phase Switching-mode Converter with ZVS

The two-phase switching-mode converter with ZVS is designed with Cadence on AMS CMOS 0.35 $\mu m$ 4-metal technology. The block circuit of whole buck dc-dc converter system is presented in Figure 5. It consists of two power buck stages, error amplifier, ramp generator, comparator and buffer stage. In the designed two-phase switching-mode converter, Pulse-Width Modulation (PWM) control technique is used.

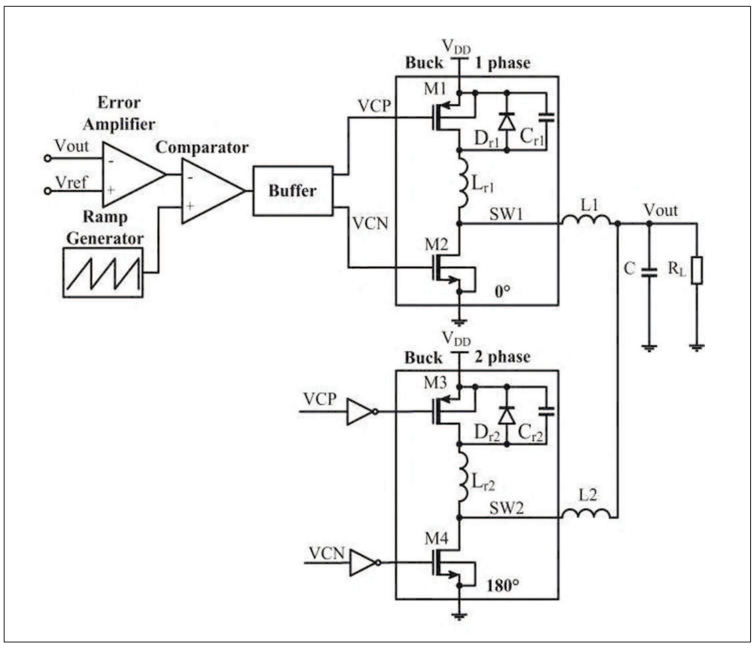


Figure 5. Two-phase switching-mode converter with ZVS

The control signals, which regulate the main power MOS transistors of the both power buck stages, are 180° phase shifted. The supply voltage $V_{DD}$ is equal to 3.6 V, which is a standard output voltage of lithium-ion battery. The average value of the output voltage $V_{out(av)}$ of the converter is regulated to be equal to 1.2 V. The output filter inductors *L1* and *L2* of the both power buck stages are equal to 125 nH. The filter capacitor *C* is equal to 400 pF. The switching frequency $f_s$ of the two-phase dc-dc converter with ZVS is equal to 76 MHz.

The PMOS transistors *M1* and *M3* in both buck power stages are represented by 6 equal "*modprf*" transistors connected in parallel. Their sizes (W/L) are respectively 150/0.35 [μm]. For NMOS transistors *M2* and *M4*, which replace the diode in the standard buck dc-dc converter circuit, 4 equal connected in parallel "*modnrf*" transistors are used. Their sizes (W/L) are respectively 200/0.35 [μm]. The values of resonant inductors $L_{r1}$ and $L_{r2}$ are equal to 10 nH. The values of resonant inductors $C_{r1}$ and $C_{r2}$ are equal to 50 pF. The waveform of output voltage $V_{out}$ of the two-phase switching-mode converter with ZVS is shown in Figure 6.

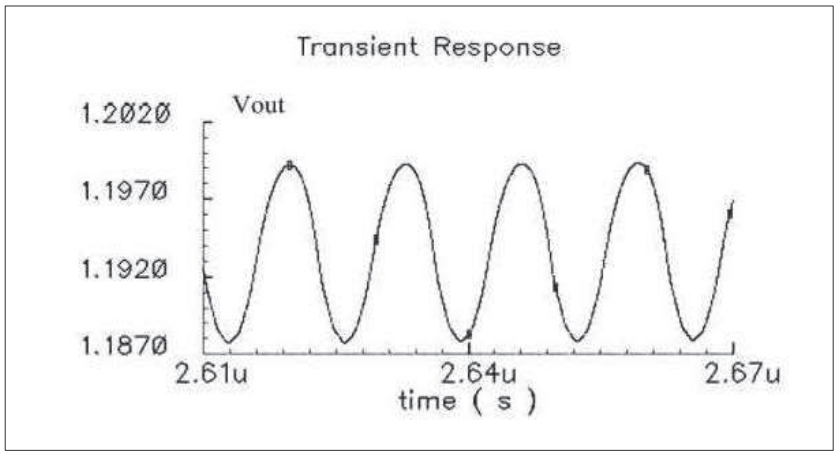


Figure 6. The waveform of output voltage *Vout* of the two-phase switching-mode converter with ZVS

The waveforms respectively of *IL1* and *IL2* of two-phase switching-mode converter with ZVS are presented in Figure 7.

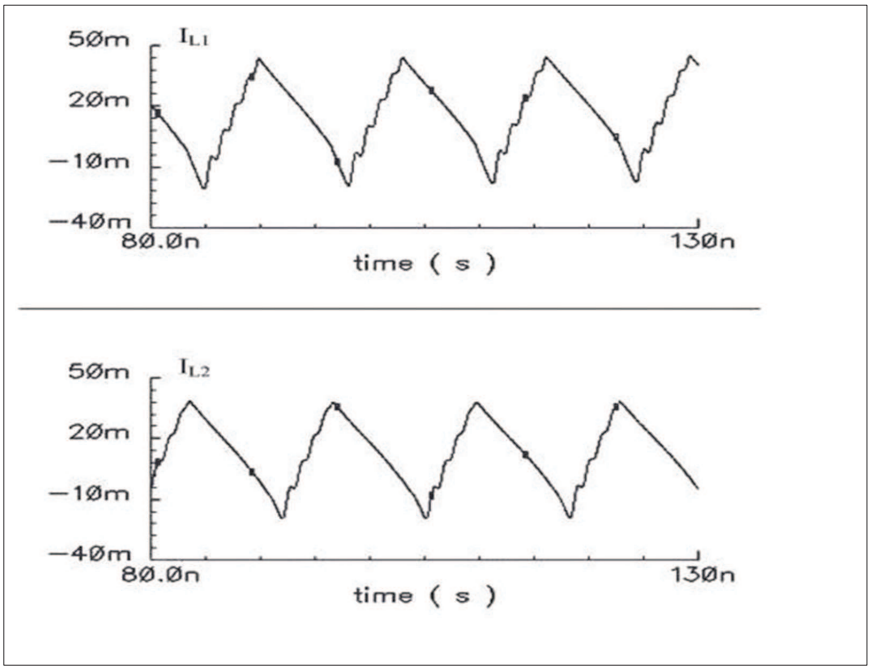


Figure 7. Waveforms of the inductor currents *IL1* and IL2 of two-phase switching-mode converter with ZVS

The waveforms of control signal *VCP*, which regulate the mode of operation of main PMOS transistors of the first buck stage, and the capacitor's voltage $V_{Cr}$ are shown in Figure 8.

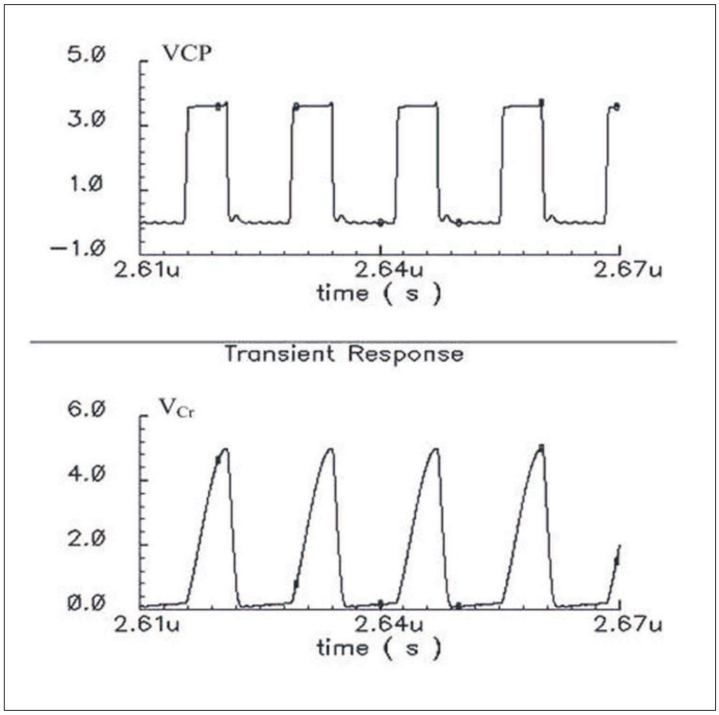


Figure 8. The waveforms of control signal *VCP* and the capacitor's voltage $V_{Cr}$

The total power losses in main PMOS transistors ($P_{PMOS}$) of two-phase dc-dc converter, designed on CMOS 0.35$\mu m$ technology, are investigated as a function of the load $R_L$. The investigations are performed when the circuit works with and without ZVS. The efficiencies of two-phase switching-mode converter, respectively with and without ZVS are evaluated. The received results are presented in Table 1.

| | $R_L$=10 [Ω] | $R_L$=20 [Ω] | $R_L$=25 [Ω] | $R_L$=30 [Ω] |
|---|---|---|---|---|
| $P_{PMOS}$ [mW] | 21.4 | 13.8 | 11.8 | 8.7 |
| $P_{PMOS}$–ZVS [mW] | 19.4 | 11.4 | 9.6 | 6.3 |
| Efficiency [%] | 67.89 | 71.25 | 74.2 | 76.84 |
| Efficiency–ZVS [%] | 69.14 | 73.43 | 76.14 | 78.26 |

Table 1. Power losses in main pmos transistors and efficiency of two-phase dc-dc converter as a function of load $R_L$, respectively with and without ZVS

All the results shown in Table 1 are received when average value of the output voltage $V_{out(av)}$ of converter is equal to 1.2 V.

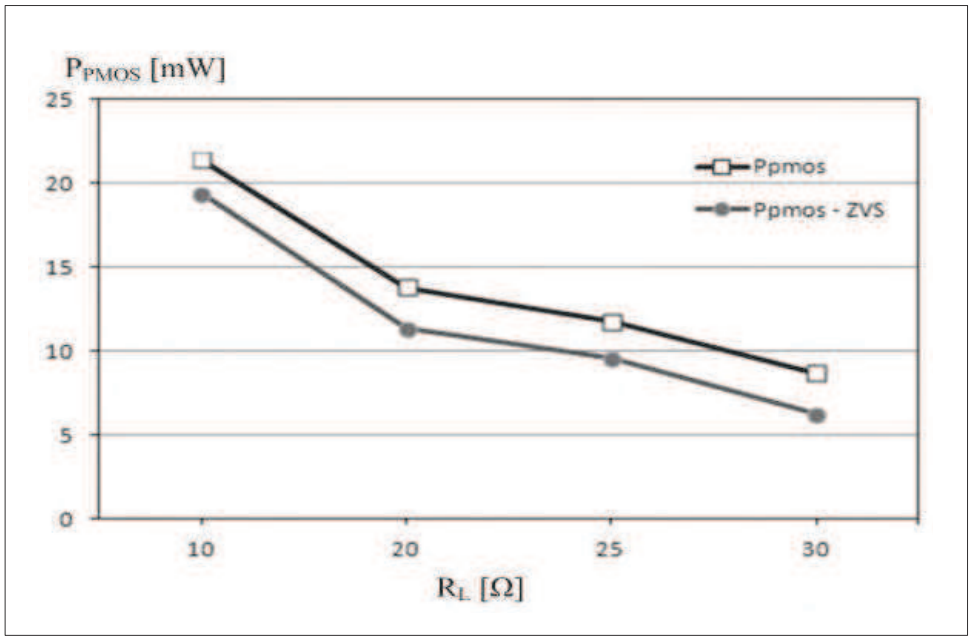


Figure 9. Power losses $P_{PMOS}$ of two-phase dc-dc converter as a function of load $R_L$ with and without ZVS

The power losses of PMOS transistors of two-phase dc-dc converter are presented graphically in Figure 9 as a function of the load $R_L$ with and without ZVS.

As it can be seen from the picture shown in Figure 9, the total power losses in the main transistors of two-phase switchingmode (*M1* and *M3*) are decreased by about 11% when ZVS technique is used. The reason is that switching power losses are minimized. This effect can be seen in Fig. 10, where the efficiency results of two-phase dc-dc converter as a function of the load *RL* are graphically presented. As it can be seen from the picture efficiency of the whole converter system is increased by about 3% when ZVS is used. The values of the load resistance $R_L$ are changed between 10 Ω and 30 Ω, because this range represents the practical equivalent value of PA used as a load [8].

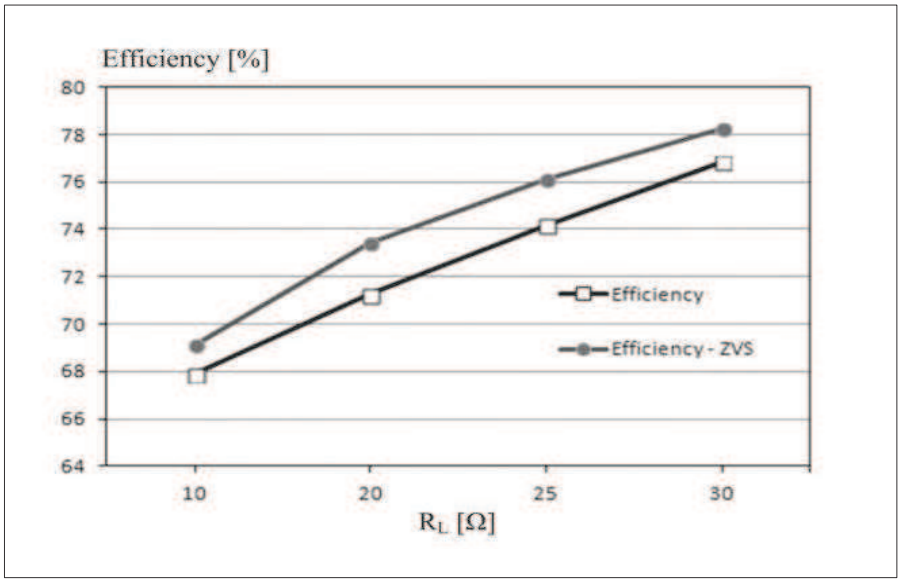


Figure 10. Efficiency of two-phase dc-dc converter as a function of load $R_L$, respectively with and without ZVS

## 4. Conclusion

In this paper two-phase buck dc-dc converter with ZVS designed on CMOS 0.35 μm technology has been proposed. This circuit could be used as switching-mode regulator in parallel hybrid envelope amplifier for LTE applications. The investigation result shows that efficiency of two-phase dc-dc converter can be increased by about 3% if ZVS technique is used. The reason is that the total losses in the main switch of the converter's power stage are minimized.

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## References

[1] Hassan, M. (2012). Wideband high efficiency CMOS envelope amplifiers for 4G LTE handset envelope tracking RF power amplifiers, University of California, San Diego, 2012.

[2] Wang, F., Kimball, D., Lie, D., Asbeck, P., Larson, L. (2007). A Monolithic High-Efficiency 2.4-GHz 20-dBm SiGe BiCMOS Envelope-Tracking OFDM Power Amplifier, *IEEE Journal of Solid-State Circuits*, 42 (6) 1271-1281, June.

[3] Li, Y., Lopez, J., Lie, D.Y.C., Chen, K., Wu, S., Yang, Tzu-Yi., Ma, Gin-Kou. (2011). Circuits and System Design of RF Polar Transmitters Using Envelope-Tracking and SiGe Power Amplifiers for Mobile WiMAX, *IEEE Transactions on Circuits and Systems I*, 58 (5) 893-901, May.

[4] Zhu, G., McDonald, B., Wang, K. (2011). Modeling and analysis of coupled inductors in power converters, *IEEE Transactions Power Electronics*, 26 (5) 1355-1363, May.

[5] Lee, J. P., Cha, H., Shin, D., Lee, K. J., Yoo, D. W., Yoo, J. Y. (2013). Analysis and Design of Coupled Inductors for Two-Phase Interleaved DC-DC Converters, *Journal of Power Electronics*, 13 (3) May, 339-348.

[6] Mohan, N., Undeland, T., Robbins, W. (2003). *Power Electronics*, *JWES, NY*, 2003.

[7] Kurson, V. (2004). Supply and Threshold Voltage Scaling Techniques in CMOS Circuits, University of Rochester, NY.

[8] Ham, J., Jung, H., Kim, H., Lim, W., Heo, D., Yang, Y. (2014). A CMOS Envelope Tracking Power Amplifier for LTE Mobile Applications, *Journal of Semiconductor Technology and Science*, 14 (2) 235-245, April.