Phase Detector, Loop Filter and Digital Control Oscillators for Control Resonant Inverters

Goran Goranov[1], Nikolay Madzharov[2]
[1]Department "Electronics" of Technical University of Gabrovo
5300 Gabrovo, 4 Hadji Dimitar st
Bulgaria
ggoranov@bitex.bg
[2]Department "Electronics" of Technical University of Gabrovo
5300 Gabrovo
4 Hadji Dimitar st
Bulgaria
madjarov@tugab.bg

ABSTRACT: *We in this work have fixed the optimal all digital PLL for the control resonant inverters. Also, we have used models to optimize the digital frequency and analysed. We then conducted experiments that find the control approach required. We have deployed the phase detector, loop filter and digital control oscillators.*

Keywords: Logic gates, Control system, PLL, CPLD

Received: 7 October 2021, Revised 2 December 2021, Accepted 11 December 2021

DOI: 10.6025/ijwa/2022/14/1/9-17

1. Introduction

The widespread use of transistor converters in various areas of practice - industry, medicine, service sector etc., imposes the new requirements to the control systems related with regulation and maintenance of certain operating modes. The implementation of the PLL functions into control systems for power converters and their investigation are presented in details in [1], [2], [3]. The use of programmable logic devices allows for the development of such systems by expanding their functionality and adaptability.

The optimization and analysis on this digital PLL give us opportunities to work in a relatively wide frequency range and small steps for adjustment. This is also and an easy connection to other digital systems. The digitally frequency synthesis is based on programmable divide a quartz stabilized frequency to obtain a change of the output frequency in a certain range and a predetermined step. There are various methods for digital frequency synthesis - a divisor of N, direct digital synthesis (DDS), I/

D - counter, fractional N, division by comparison schemes, etc. They are hardly realizable in a discrete implementation [4], [5], [6].

The analysis of digital PLL is limited to the examination of each module separately - Figure 1.

In the previous studies and researches of the author feasibility of a digital PLL, using I/D - counter and FRACTIONAL N method are affected. The conclusion is that various digital controlled generators require a substantial change in the functions of the previous blocks in the digital PLL. Often this refers to the digital filter, which is connected to the generator. Phase detector in most of the cases does not change unless you change monitoring requirements for the phase difference. Figure 1 shows a digital PLL, comprising a phase detector DPD, converting the phase difference into a signal of a specified duration, the digital filter DLF, converting the signal from the phase detector and the digital controlled oscillator DCO. In operation of the system, frequency Fout of the output signal of the DCO seeks to achieve input frequency Fin with certain accuracy. The change of the input frequency Fin generates an increase or decrease of the phase difference between it and the output frequency Fout, which leads to their alignment (Fin = Fout).

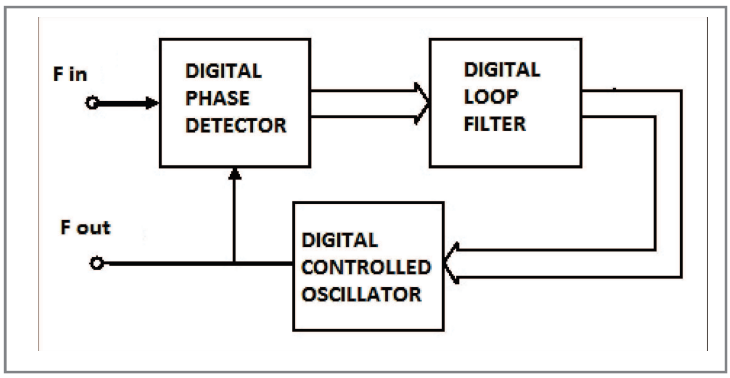

Figure 1. ALL digital PLL

2. Synthesis of the Basic Modules

Phase Detector

The most felicitous for use from the three main types of phase detectors (XOR, JK-Flip Flop and frequency phase detector) in the management scheme of the resonance inverters is the frequency phase detector. This is a detector with three states, managed by the front of the input signal. The range is ± 360 ^{o}. From the timing diagram shown in Figure 2 we can see the advantage of the phase frequency detector. In phase difference φ = 0 signals UP and DN are also zero. Depends on the direction of the phase shift, in one of the two outputs, is obtained the pulse *K*3, proportional to the phase difference.

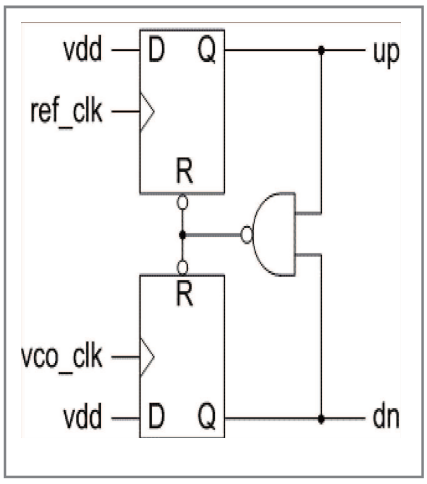

Figure 2 a)

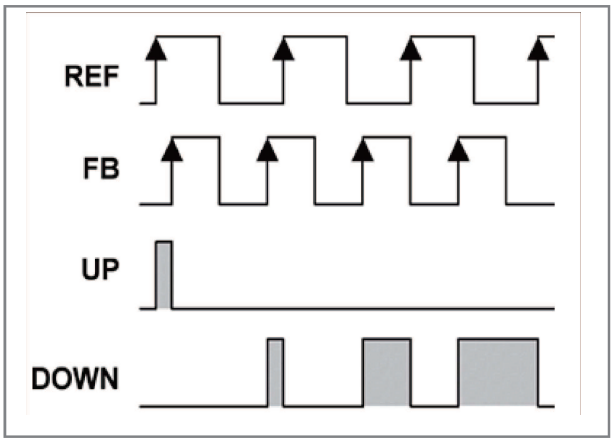

Figure 2 b)

Digital controlled oscillator

FRACTIONAL - N

The block diagram representing the method consists of two main blocks for division of an integer and a fractional part - Figure 3.

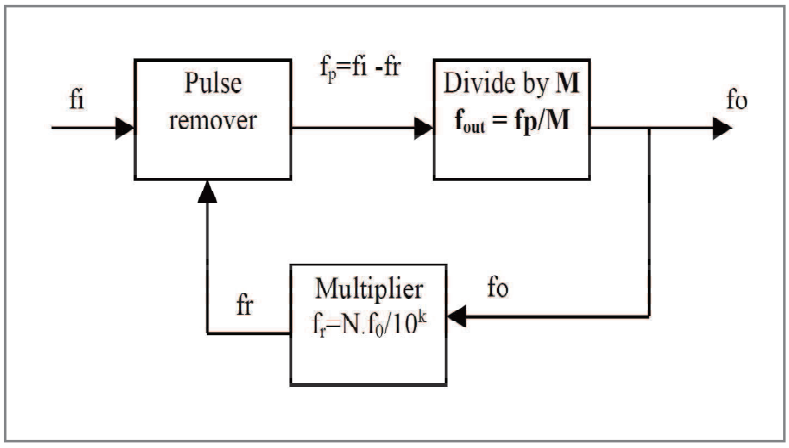

Figure 3. Basic Fractional-N

The input clock frequency f_i is used. Part of the pulses is removed in reducing impulses block. The number of the removed pulses is proportional to the ratio N, issued by the block of the multiplier. The removal of the phase noise (asymmetry between successive pulses) is achieved most easily as "blur" in time. The division factor M is used, which is an integer - block divider of M. The output frequency is calculated by the following formula

$$f_{out} = \frac{f_p}{M} = \frac{f_i - f_r}{M} = \frac{f_i - \frac{N.f_{out}}{10^k}}{M}, \quad (1)$$

from where

$$f_{out} = \frac{f_i}{M + \frac{N}{10^k}}, \quad (2)$$

$$f_{out} = \frac{f_i}{M + \frac{N}{10^k}} - \frac{f_i}{M + \frac{N-1}{10^k}}, \quad (3)$$

In the presented formulas M is an integer, K is number of decades, and N is an integer in the range of 0 to $10^k - 1$. On this basis, for the realization of FRACTIONAL - N method are needed binary decimal counters for M divider and multiplier for divisor N. If the coefficient of division M varied from 0 to 9, you will need a counter with two digits of M i.e. an amendment from 0 to 99, respectively, two counters and etc. The same goes and for the divisor N, which determines the fractional part. For example in the number of decade $K = 2$ is obtained by dividing the frequency 1,00 to 99,99 .

The implementation of the digital Fractional-N divider for management of the resonant inverter has the following advantages and disadvantages:

- Works in a wide frequency range.
- Receives relatively low phase noise and hence little impact on the optimal operation of the power transistor converters.
- Easy to implement coordinating digital filter

Disadvantages:

- Nonlinear step of modifying the frequency - depending on the divisor.
- Receives relatively low phase noise and hence little impact on the optimal operation of the power transistor converters.

DDS – generator

DDS – generator is a type of generators, which is driven by a digital code (word), called the DCO. It works with digital converter filter time-digit code. On Figure 4 is shown the block structure of this type of frequency synthesis.

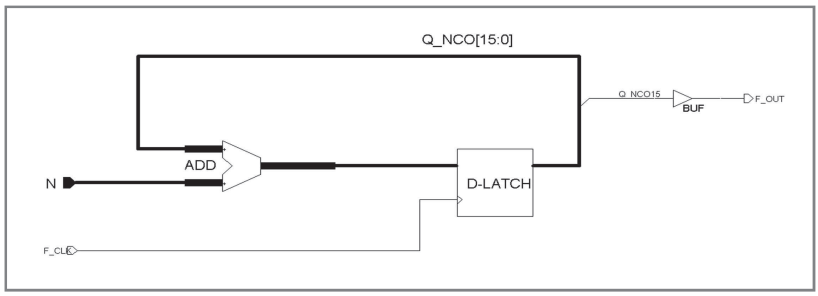

Figure 4. DCO

The output frequency is given by:

$f_{out} = f_{clk} . N/2^k$ (4)

where 2^k is the sparsity of the ADD.

The amendment of f_{out} varies from 0 [Hz] to $f_{clk}/2$ [Hz] with step:

$\Delta f_{out} = f_{clk}/2^k$ (5)

Advantages and disadvantages of using DDS method for managing resonant inverters are:

- Working in a wide frequency range max ½ fin.
- A very small step of frequency variation -Δf .
- Easy to implement digital matched filter.

Disadvantages:

- The main disadvantage is the phase noise, its value reaches *1/f,* at *fout=1/2fin.*
- Requires large program capacity.

Increment/decrement counter

This is a bias scaler, whose amendment is managed by two entrances carry and borrow - figure 5.

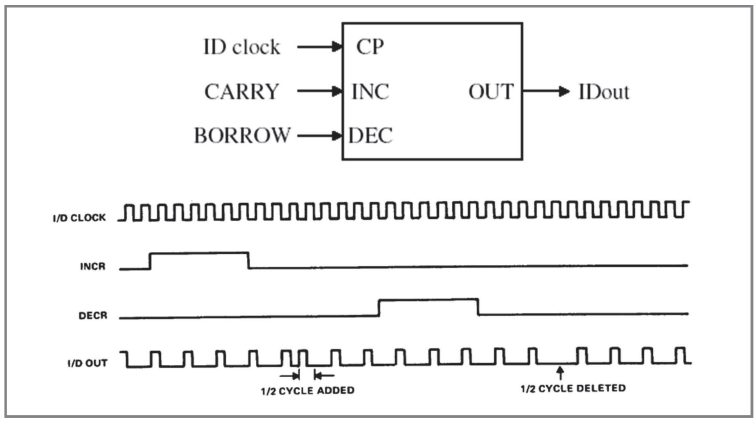

Figure 5. I/D – counter and timing diagram

The resulting output frequency (I/Dout) of I/D counter – is ½ I/Dclk. It may be amended "up" or "down" depending on which input is received 1-0 transition. The amendment is obtained by adding or deleting ½ cycle. To reduce the phase noise can be used an additional counter (divisor N), then phase noise will be reduced by 1/N.

Advantages and disadvantages in using this method are:

« Relatively small step of frequency variation - Δf (tens of Hz).

« Small phase.

Disadvantages:

« Complex to implement digital filter

« Limited range of frequency variation

« Dependence on many parameters.

Loop filters.

The task of the filters is to convert the signal so that it is convenient to control the synthesized oscillator. Depending on the digital synthesized adjustable generator are used various filters. If the used generator is I/D – counter, then a filter that converts the signal phase difference from the phase detector in the number of pulses is needed. Thus plays the role of an integrator [8].

Such a filter can be realized by a reversible counter with an adjustable division ratio, called K-counter - Fig. 6. The principle is explained with tim diagrams shown in Fig. 7. The number of output pulses (transfers) is proportional to the operating time of the respective counter UP or DOWN, respectively, and the phase difference.

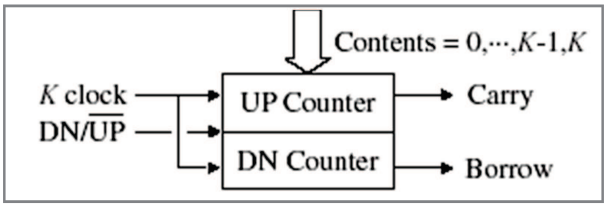

Figure 6. Programmable frequency divider of K - counter

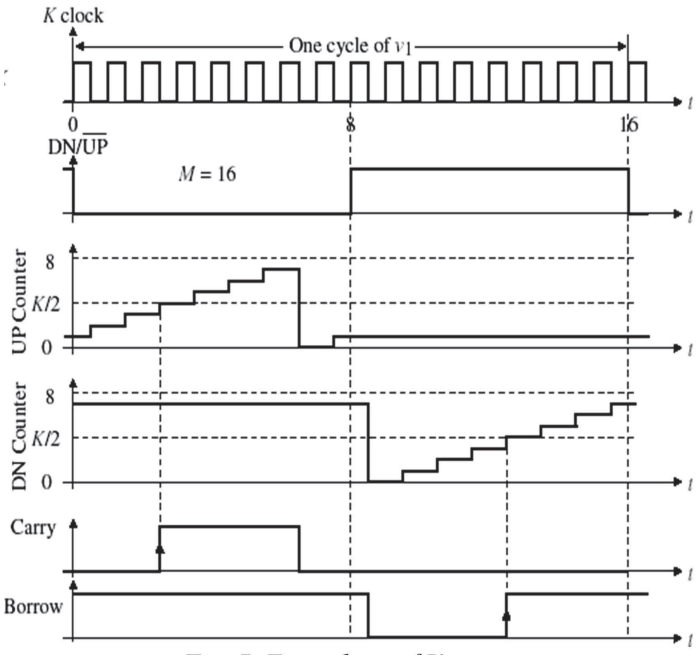

Figure 7. Time chart of K – counter

Another type of filter is converter of time into a digital code. The resulting code (word) N directly operates the generator - DDS or Fraction-N, changing its output frequency proportional to the code N. The condition for synthesis of the converter is f_{clk} >> EVENT.

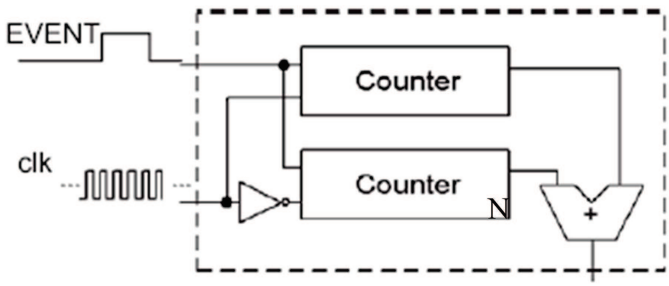

Figure 8. Converter time numerical code

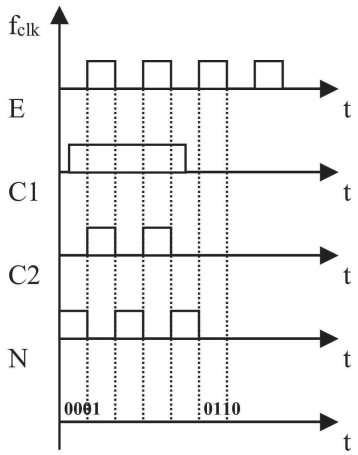

Figure 9. Time chart of converter - time in numerical code

Between the considered options are development and synthesized PLL scheme with DDS generator and filter T2C (time to code converter) in CPLD Xilinx CoolRunner2.

The experimental object for management is a transistor half-bridge parallel inverter, which is running with frequency above the resonance one. The input power of the converter is P = 1, 6 kW. Load capacitance value is C = 1,72 μF. It is implemented with non-inductive capacitors. The load inductance - the inductor has a value L = 3,1 μH, wound copper tube with a diameter of 9 mm with 13 windings. The diameter of the inductor is 73 mm.

A study of system performance under different input power and loads has been made. On Fig. 10 a) is shown the current and voltage in resonance at low load and input voltage E = 130V and input current I = 12,3A. On the channel one of the oscilloscope is visualized the form of the current and on the channel two the form of the voltage. Both signals were observed after the transformers for feedback. It can be seen that the mode of the inverter is good, when the frequency is maintained by digital PLL. The increase of the input voltage leads to bigger power load. This will lead to its heat and therefore to change the parameters of the circle and therefore the frequency will start to decrease.

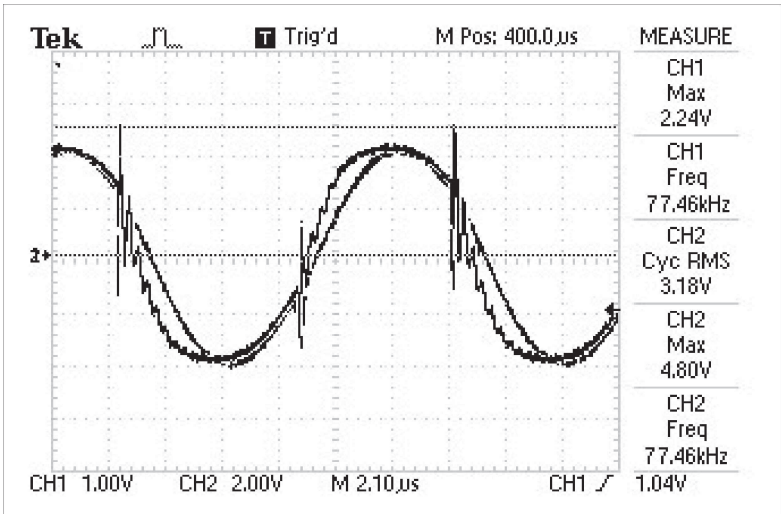

Figure 10 - A) Voltage on the parallel circuit and the current - hollow material

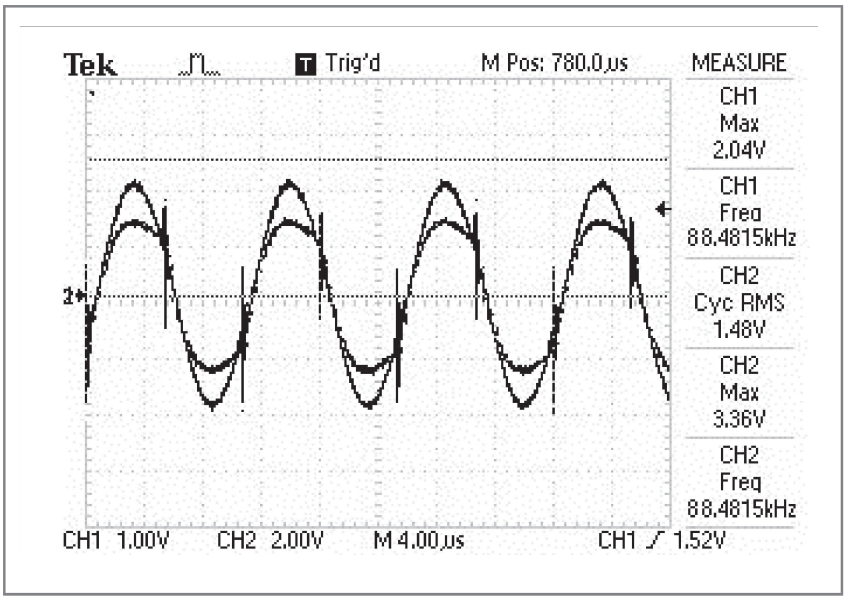

Figure 10. B) Voltage on the parallel circuit and the current - dense material

At higher load (when solid material is used), the operating frequency is changed on 88,48 kHz - Figure 10 b). Input voltage E = 122V, I = 10, 7 A.

3. Conclusion

The analysis shows that the best results are achieved when synthesized management scheme with 16bit DDS generator is used. A 16 bit counter for filter, which converters signal from the phase detector is realized. The response time of the system as a whole depends on the sparsity of the filter and the time of integration. Time integration is proportional to the signal EVENT - phase difference. Under the process of locking frequency (resonance inverter) phase deviation is small and therefore the reaction has several clock cycles. Great importance has the supporting clocked. Although the inverter operates at frequencies from 60 to 100 kHz by using 50MHz reference frequency. Thus the influence of phase noise is minimized.

Good results are achieved also when I/D counter is used, but the digital filter is more complex and requires more programmable logic resources. Using methods for fully digital control improved adaptability to any electronic system, provide much easier monitoring of parameters and setting of such microcontrollers.

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