An Interface Architecture of Source-Synchronous Differential Point-To-Point Parallel Link

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ABSTRACT: *To transmit parallel data is normally we use clock across printed circuit board so that the skew problem is addressed. The issue is that the phase relation of the data and clock can be a failure due to different travel times through the link. We fixed the issue with an interface architecture of source-synchronous differential point-to-point parallel link. We used in this work an effective clock de-skew structure based on Delay Locked Loop. It is applied in the BiCMOS technology and is described with a low successful case locking time 40 ns (20 cycles @ 500 MHz), with other features.*

Keywords: Differential Interface, Clock Skew, Transmission Line, DLL

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1. Introduction

With the rapid advances in modern VLSI IC technology synchronous data transfer between PC boards, at rates of order up to several gigahertzes, is required. The need for high inputoutput bandwidth has led to widespread use of differential signaling. In essence, a differential pair is realized with two transmission lines that have equal and opposite polarity signals propagating on them, so that the positive path and the negative path (of a differential pair) are tightly timed [1]. However, in practical realizations there are differences between two signal paths. The differences are primarily imposed by unequal signal path length routing, local variation of the epoxy laminate dielectric constant, unmatched twists or kinks in the link connections, etc. As a consequence, all these differences can cause positive and negative paths to deliver their signals at different moments at the end of a differential channel, i.e. to provide signal skew, also called within-pair skew or intra-pair skew, what at different locations may degrade system performance, and even cause system malfunction. To remedy for within-pair skew in PCB traces, system design engineers use dielectric materials construction with a mixture of fiber and non-fiber, while for de-skew compensation (correction) in cables they choose customized cables and connectors. However, the system cost of those solutions is very high [2-4].

In this paper we propose an electronic within-pair de-skew solution intended for automatic align of two signals in a differential pair at the receiver. This electronic is part of the source-synchronous point-to-point parallel link interface intended for high-speed differential data transfer over PCB. It is DLL based circuit which samples the delay differences from both the positive and negative edges of the reference clock signal and is characterized with fast locking time, wide bandwidth, and small static phase error.

2. Problem Definition

During the last three decades, with the incredible rapid advance of MPU's operating frequency, memory and inputoutput subsystems are required to keep-up by increasing clockdistribution and data-transfer speed. The need for high memory/input-output (I/O) bandwidth has led to the widespread use of point-to-point parallel links. Conventional parallel links are generally source-synchronous with a clock sent along with data signals for receiver timing recovery, i.e. high speed system interfaces usually transmit a high speed clock synchronously with a parallel data stream [4].

2.1. Transmission Line Delay, Theory

We will explain now, in short, the used theoretical aspect for skew estimation (timing difference between signals) in terms of signal path difference and dielectric constant [5]. Phase velocity of signals on transmission line, v_p, have a form:

$$v_p = \frac{1}{\sqrt{\mu \cdot \varepsilon}} = \frac{c}{\sqrt{\mu_r \cdot \varepsilon_r}} \cong \frac{c}{\sqrt{\varepsilon_r}} \tag{1}$$

where c is the speed of light, μ_r relative magnetic permeability, ε_r relative dielectric permittivity. On standard PCB, based on FR4, as most commonly used composite material, μ_r is 1 and ε_r is in the range from 4 up to 4.4. When the signal path on the PCB changes for

$$\Delta l = l_1 - l_2 \tag{2}$$

at transfer speed

$$v_p = \frac{\Delta l}{t_{delay}} \tag{3}$$

produces a delay that can be estimated based on the effective dielectric constant (for the FR4-based PCB typically $\varepsilon_{r\,eff}$= 3.4). The delay calculated as

$$t_{delay} = \frac{\Delta l}{v_p} = \frac{\Delta l}{c} \cdot \sqrt{\varepsilon_{r\,eff}} = \frac{1\,\mathrm{m}}{3\,10^8 \frac{\mathrm{m}}{\mathrm{s}}} \cdot \sqrt{3.4} \tag{4}$$

and the resulting value is t_{delay} = 6.15 ns/m, i.e. t_{delay} = 61.5 ps/cm. This implies that Δl = 1 cm can cause serious problem in clock synchronization.

2.2. Source-synchronous Point-to-point Parallel Link Interface

Typical source-synchronous unidirectional and differential point-to-point parallel link interface architecture [3], is presented in Figure 1.

Notice: CLK_{REF} stands for referent clock signal; TxCLK (RxCLK) –global transmitter (receiver) clock signal; TxCLK_Gen (RxCLK_Gen) – transmitter (receiver) clock generator; DCB - differential clock buffer; DTB_0,…, DTB_{n-1} (DRB_0, …, DRB_{n-1}) - differential transmitter (receiver) data buffer; DLL-CLK-Skew_Compes. – delay locked loop skew compensator; D_0, …, D_{n-1} – data signals

All data signals (D_0,…, D_{n-1}) and a referent clock signal CLK_{REF} are transmitted synchronously. Data rate of signals D_0,…, D_{n-1} is determined by TxCLK (RxCLK). At the receiver, a delay locked loop skew compensator (DLL-CLKSkew_ Compes) generates referent clock signal CLK_{REF}, while the receiver clock generator RxCLK_Gen generates a global receiver clock RxCLK. The RxCLK is used to sample all incoming data signals D_0, …, D_{n-1}. Correct sampling is achieved when TxCLK = RxCLK.

Here in focus of our interest is the design of DLL-CLKSkew_ Compes as constituent of the system presented in Figure 1. Design of other building blocks (sketched in Figure 1) is currently under further investigation and is directed towards development of bidirectional parallel link interface.

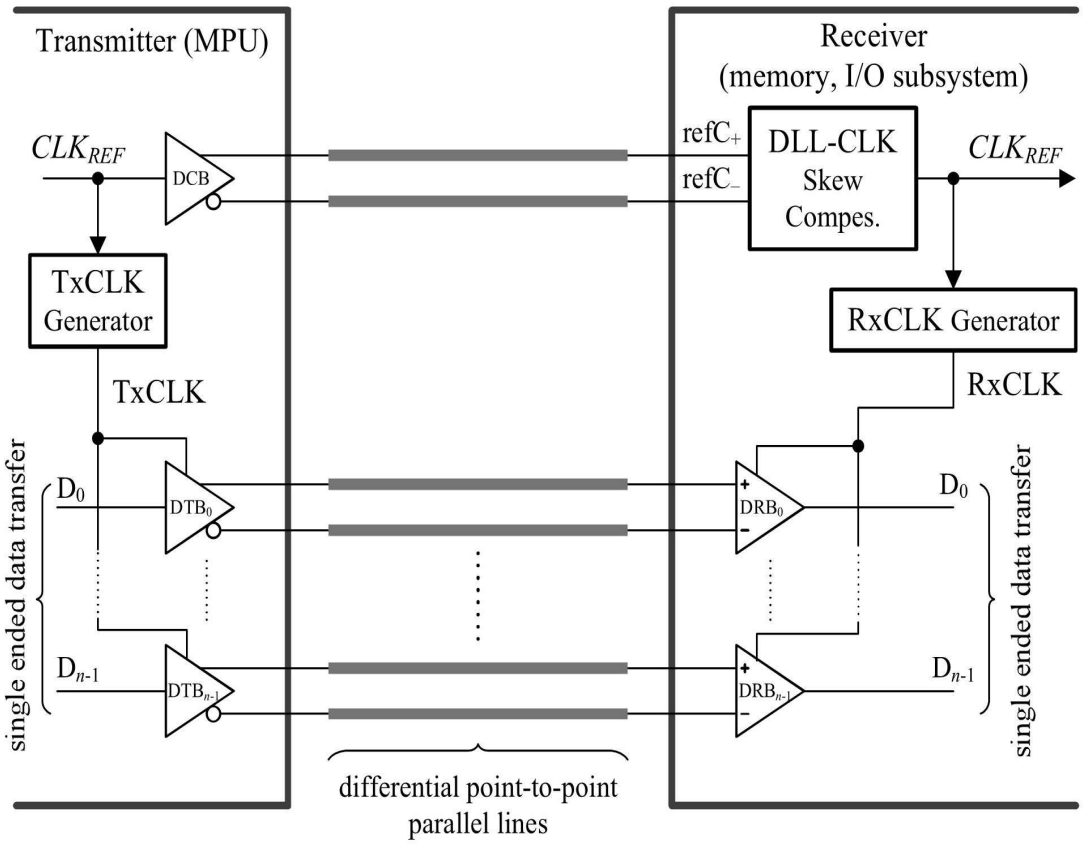


Figure 1. Source synchronous simultaneous unidirectional and differential point-to-point parallel link interface architecture

3. Delay Locked Loop Clock Skew Compensator Architecture

The timing difference between signals is called skew. It mainly arises from signal trace incongruity such as trace-length difference in PCB or on the memory and I/O modules, unequal parasitic elements of the packages, etc. Data bus skew have critical impact on the whole performance of the memory and I/O subsystems at over 100 MHz clock period [1-4]. To solve this problem in an efficient manner, clock de-skew electronics is used. In general, Phase Locked Loops (PLLs) and Delay Locked Loops (DLLs) are broadly used in high-speed digital systems, clock synchronization and data recovery systems. Figure 2 shows the architecture of the DLL-CLK Skew Compensator. As can be seen in Figure 2 this system building block consists of a phase-frequency detector (PD), a loop filter (LF), and a voltage controlled delay line (VCDL), and inverter. The PD is an important component in designing DLL based structure [6].

It detects the phase error information between input reference signal refC+ and generated signal refC- generated output by VCDL. Phase error information is generated in the form of UP and DOWN signals. The produced signal by PD is sent to CP. To adjust the delay of VCDL, CP and LF (integrator) generate appropriate value for control voltage of VCDL (marked as V_{ctrl}) based on the phase difference of *refC+ and *refC- signals.

4. The Proposed Phase Detector Architecture

The PD sketched in Figure 3 represents crucial component of the DLL-CLK Skew Comp building block. The transistor schematic of a phase detector sensitive both to positive and negative clock edge transitions is presented in Figure 3(a). The PD consists of two blocks intended to handle the input signals *refC+ and *refC . Each block is composed of two stages, pprecharge (n-precharge) and n-precharge (p-precharge), connected in cascade, followed by an inverter (buffer). The PD operation principle is depicted in Figure 3(b). As can be seen from Figure 3, the widths of UP and DOWN signals are proportional to the phase

difference between the *refC+ and *refC signals. Waveforms in the left side of Figure 3(a) represent the case *refC+ leading *refC , while those given in right side of Figure 3(b) to the case *refC leading *refC+.

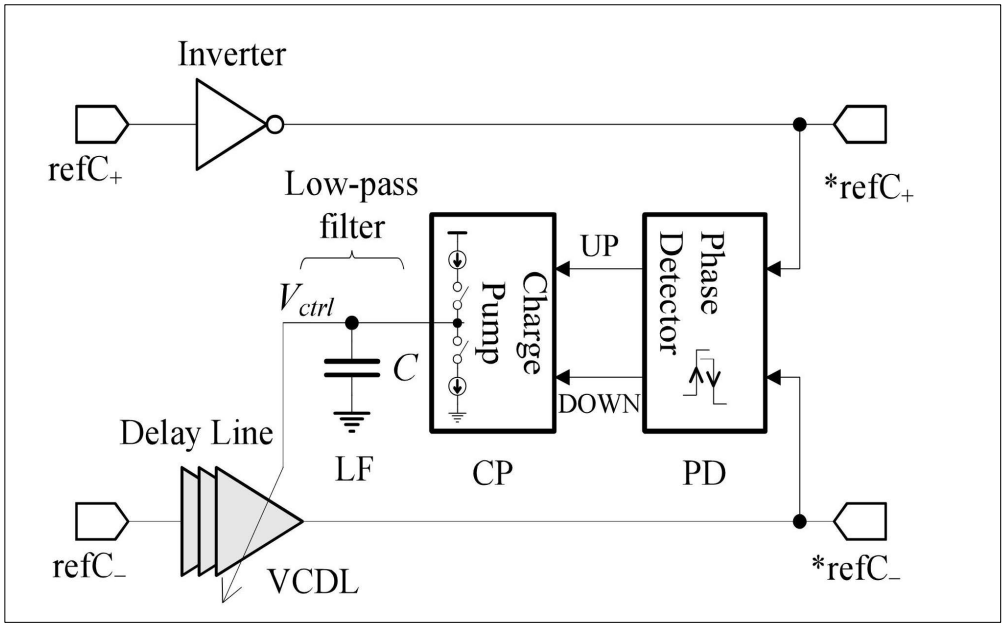
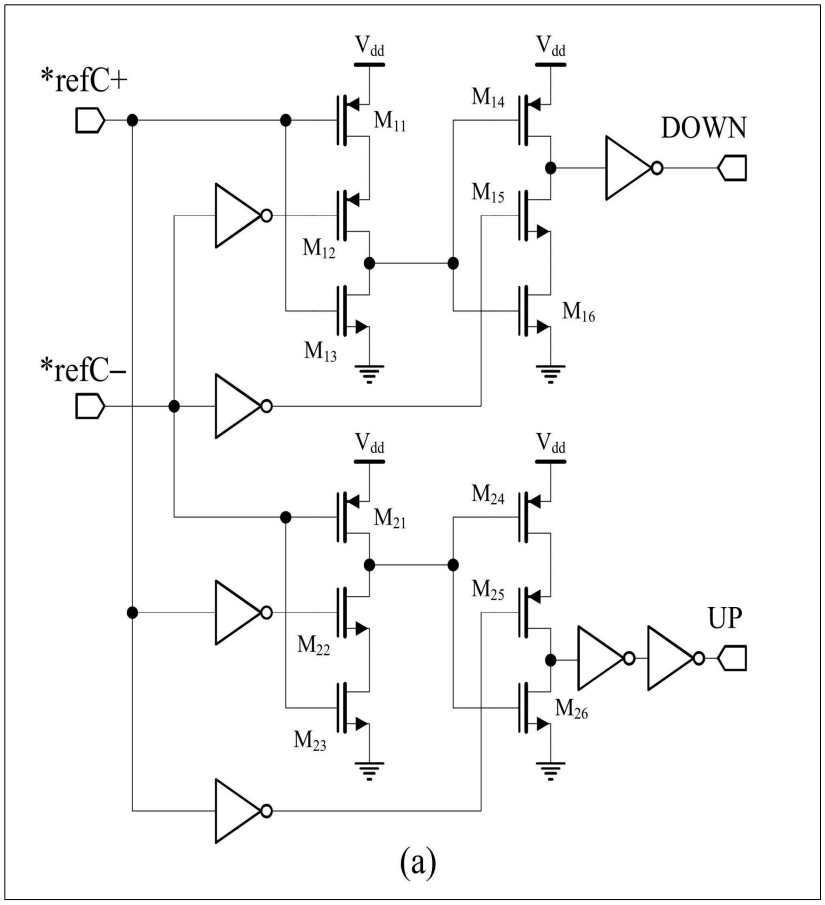


Figure 2. Architectural structure of the delay locked loop clock skew compensator



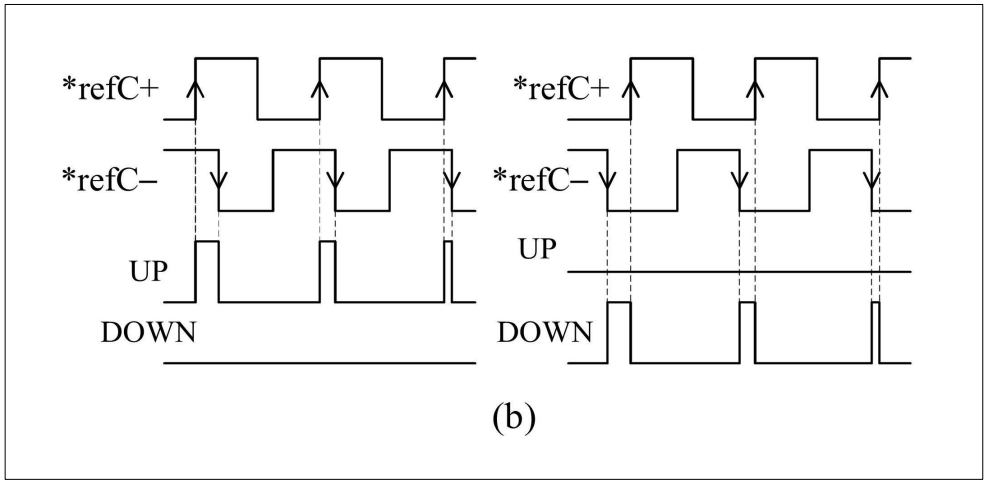


Figure 3. PD transistor schematic (a), waveforms of PD (b)

5. Charge Pump

In the DLL structure given in Figure 4, the phase error between the input reference clock and the VCDL output clock is sensed by the PD and transferred to the CP in the form of voltage pulses. The CP performs the function of adjusting the voltage of the LF and thereby altering the VCDL delay according to the phase error information from the PD. In principle, the CP simply consists of two controlled switches, one current source (transistor M3), and one current sink (transistor M2), as shown in Figure 4. Transistors M1 and M4 are used as switching elements. The LF is realized with the capacitor C which acts as an integrator.

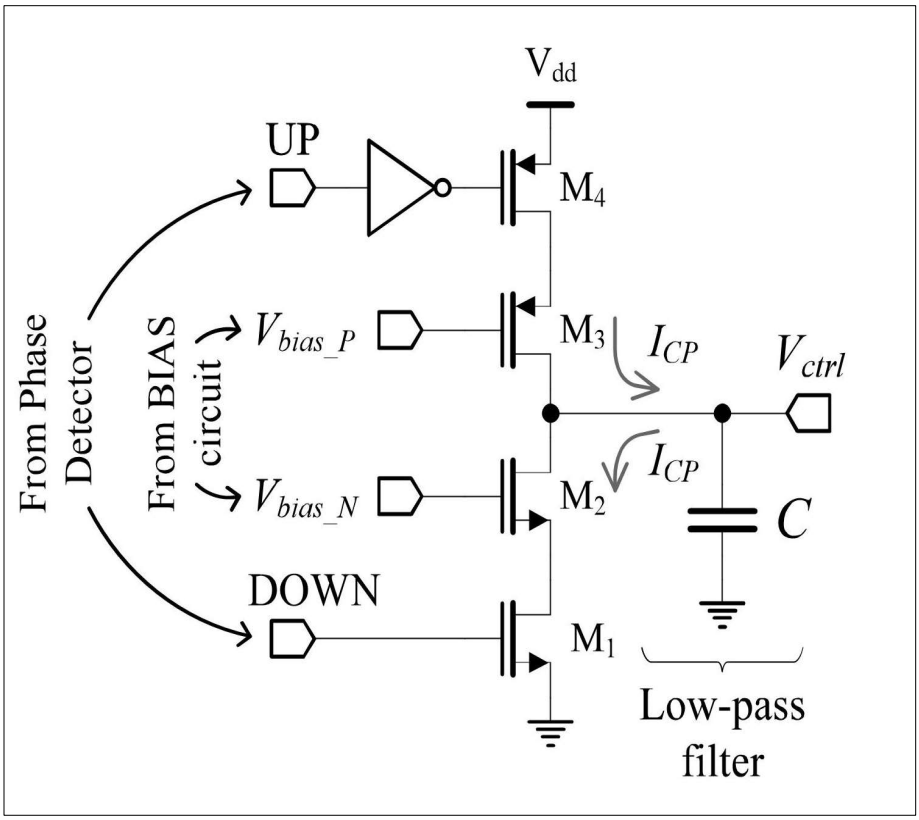


Figure 4. A simplified charge pump schematic

6. Voltage Controlled Delay Line

The output signal of the DLL is directly taken from the VCDL. The proposed VCDL consists of six delay stages (cells) which are connected in series. The total delay of the VCDL is equal to one clock period CLK_{REF} (or a phase shift of 360°) in the locked state. Theoretically, all the delay stages in the VCDL are identical, and each delay stage contributes a time delay of CLK_{REF} / 6 for six-stage VCDL. Let note that, the number of delay stages is adjusted in accordance with the operating frequency. Using more stages increases the phase resolution, but also increases the minimum VCDL delay. The structure of the VCDL delay stage is presented in Figure 5. At the left part of Figure 5, the bias circuit of VCDL is presented, and on the right side circuit structure of a single delay stage is given [7].

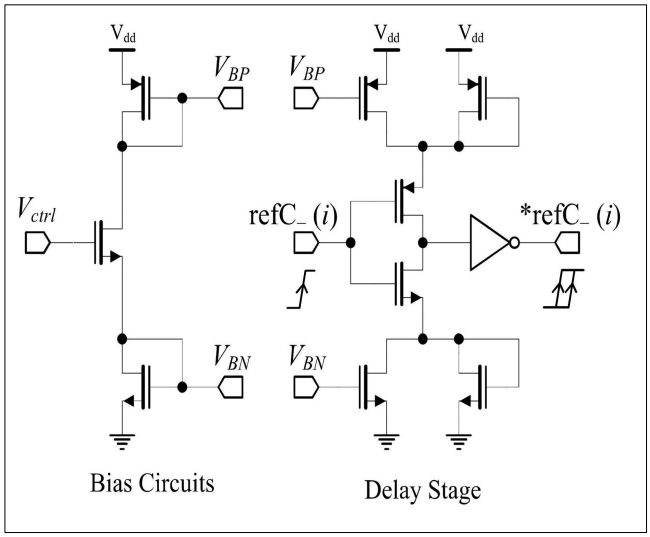


Figure 5. VCDL delay stage

Operation of the six stage delay line is simulated and the obtained result which corresponds to the total time dependency in terms of control voltage is sketched in Figure 6.

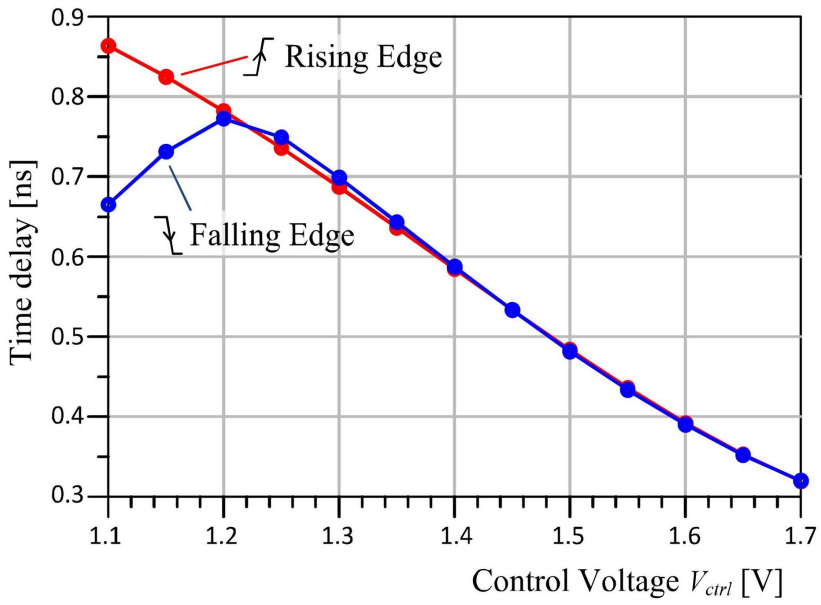


Figure 6. Time delay variation in terms of control voltage

7. The PD & CP Characteristic

There are several important characteristics concerning PD & CP, but one having the largest impact is the output phase characteristic, i.e., the PD & CP output current vs. phase error [6]. Fig. 7 illustrates the phase characteristic for the proposed PD & CP architecture. As can be seen from Fig. 7 the phase characteristic is dominated by two issues, dead-zone and blindzone. In our design solution the dead-zone is minimized thanks to the fact that the proposed PD architecture does not utilize intermediate signals for reset operation, as is the case in conventional PDs, but rather generates UP and DOWN signals directly. With the proposed circuit topology, the PD architecture achieves a small blind-zone close to the limit imposed by dynamic characteristics of MOS transistors and parasitic capacitances of internal nodes.

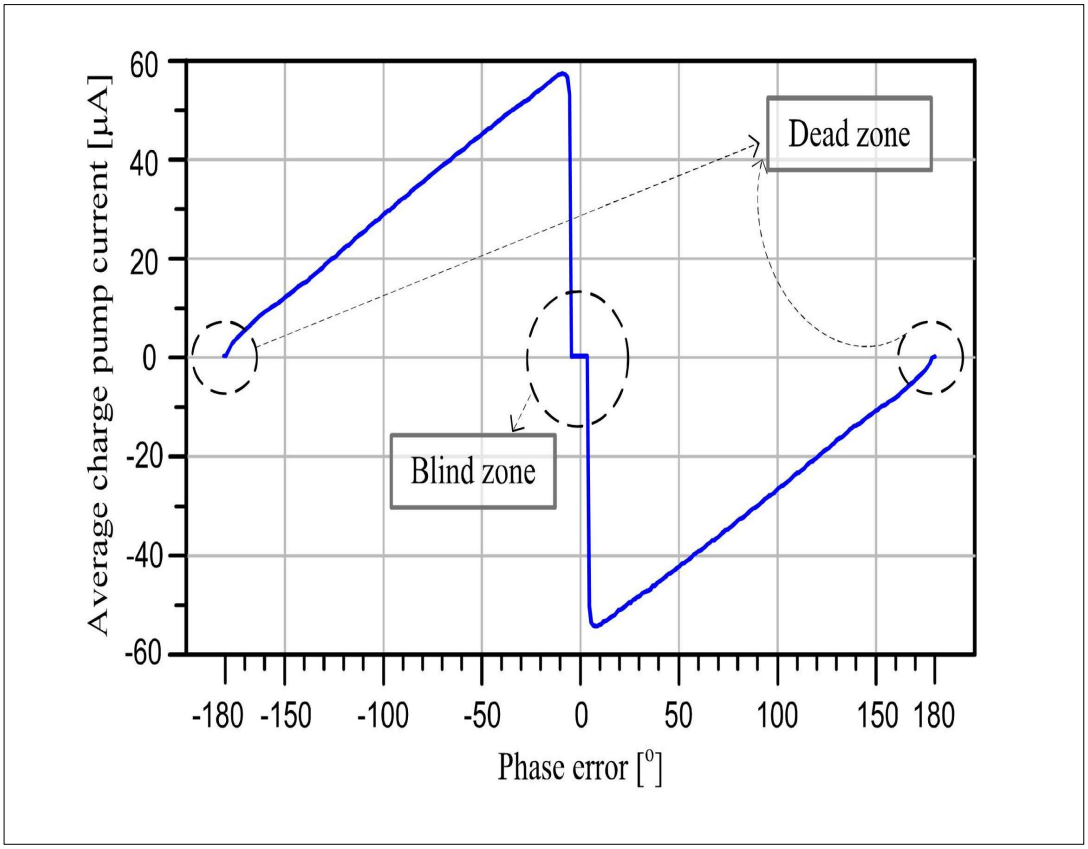


Figure 7. Phase characteristics of PD

The maximal operating frequency of PD was determined by measuring rising-, falling-, and hold-time of the UP (DOWN) signal obtained at the output of the circuit. Rising- (falling-) time deals with time period during which the pulse amplitude variation are within a range from 10% up to 90% (from 90% down to 10%). Hold time correspond to the needed time for charging (discharging) parasitic precharge capacitors. During this, the worst case technology corner was selected for performance evaluation. By summing the obtained parameters, the maximum operating frequency was determined. In our case it was 8 GHz.

8. Simulation Results

In Fig. 8 the transient response of the DLL-CLK Skew Compes (from Fig. 2) constituent is given. As can be seen from Fig. 8. after powering-up the DLL-CLK Skew Compes enters into locking state after 40 ns what correspond to 28 clock cycles at operating frequency of 660 MHz. In the locked state, the voltage (charge) of the loop filter is kept constant. It is possible that equal charging and discharging will still happen in the locked state. In fact, it is desired to have such activities to minimize jitter. However, the charging and discharging currents must be identical as well as very narrow so that the voltage of the loop filter will not be disturbed.

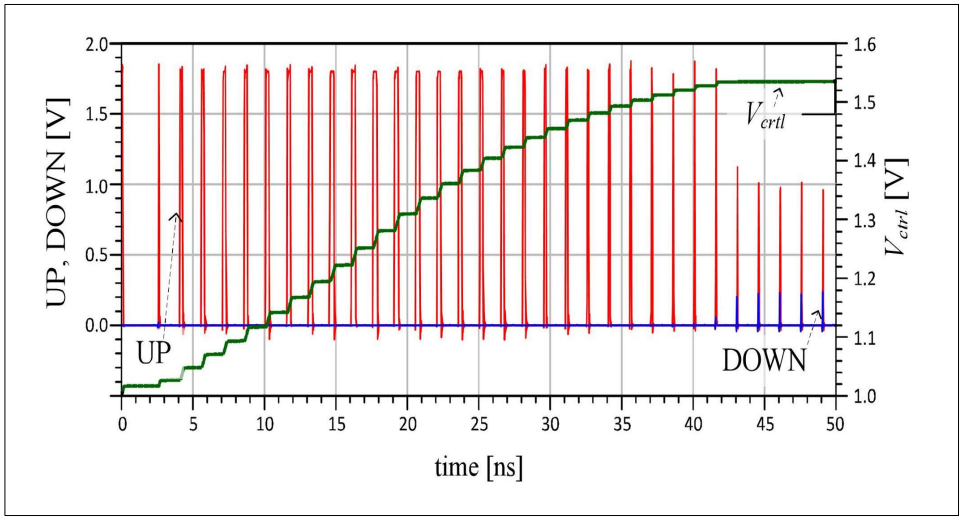


Figure 8. Transient response of DLL-CLK Skew Compes

In Figure 9, waveforms at the inputs refC+ and refC- and outputs *refC+ and *refC of DLL-CLK Skew Compes building block are presented. As can be seen in Figure 9, in locking state, the estimated static phase error is very small (~7 ps).

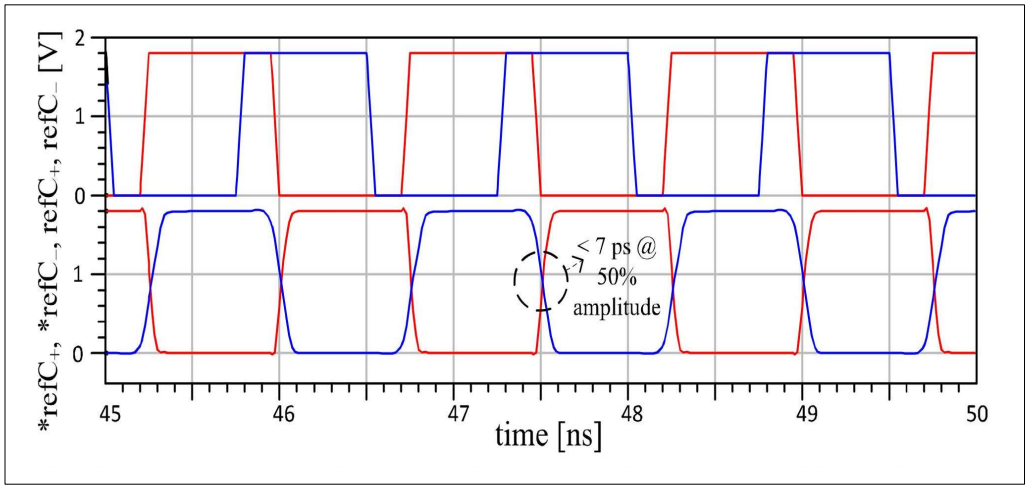


Figure 9. Waveforms at inputs and outputs of DLL-CLK Skew Compes

The presented results are obtained by using Advance Design System software tool with IHP design kit for 0.13 m BiCMOS technology [8].

9.. Conclusion

Clock skew represents crucial problem in designing source-synchronous unidirectional and differential point-to-point parallel link interface architecture. In this paper an efficient Delay Locked Loop clock de-skew compensation-based architecture is described. The proposed circuit is implemented in IHP 0.13 pm BiCMOS technology [8]. It has fast locking time 40 ns (20 cycles ® 500 MHz), wide lock frequency range from 470 MHz up to 870 MHz, and static phase error of 7 ps.

Acknowledgement

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References

[1] Ritchey, L.W. (2008). A Treatment of Differential Signaling and Its Design Requirements. Speeding Edge: Glen Ellen, CA, USA.

[2] Zheng, Y. & Liu, J. (2011). A 5 Gbps Automatic Within-Pair Skew Compensator for Differential Data in 0.13 mm CMOS. *IEEE Transactions on Circuits and Systems*-1, 58, 1191–1202.

[3] Ryu, K., Jung, D.H. & Jung, S.-O. (2012). A DLL with dual edge triggered phase detector for fast lock and low jitter clock generator. *IEEE Transactions on Circuits and Systems*, 59, 1860–1870 [DOI: 10.1109/TCSI.2011.2180453].

[4] Yeung, E., Horowitz, Mark. (2000). A 2.4 Gbps/Pin Simultaneous Bidirectional Parallel Link with Per-Pin Skew Compensation, *IEEE Fount & of Solid-State Circuits*, Vol. 35, pp. 1619–1628.

[5] Ludwig, R., Bogdanov, G. & R.F. Circuit design: Theory and applications, Sec. CD. Prentice Ilall. NJ, USA (2009).

[6] Nikolic, G. & Jovanovic, G., Stojcev, M. & Nikolic, T. (2017) Precharged phase detector with zero dead-zone and minimal blind-zone. *Journal of Circuits, Systems and Computers*, 26, 1750179 (16 pages) [DOI: 10.1142/S0218126617501791].

[7] Jovanovic, G.S. & Stojcev, M.K. (2006) Current starved delay clement with symmetric load. *International Journal of Electronics*, 93, 167.175.

[8] HIP-Microelectronics SiGe:C BiCMOS technologies for MPW & prototyping. https:// www.ihp-microclectronics.com/en/servicesImpw-prototyping/sigerebiernos-technologiechtml.