Performance Analysis of the Circuit Simulation with MOSFET Transistors

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ABSTRACT: *In this study we have presented the analysis of the channel effects of MOSFET transistors. We also did performance analysis of the circuit simulation with MOSFET transistors. The purpose of this work is mainly for educational methodology aspects.*

Keywords: Short Channel Effect, MOSFET Transistors, Analog Circuits

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1. Introduction

The presented paper is aimed toward educationalmethodological purposes. The contemporary high level of miniaturization requires that by the electronic design all possible factors should be considered. The short channel effects are very widespread in MOSFET devices. They can be summarized in the following directions[1]: channel length modulation; threshold voltage roll-off; narrow gate width effects; reverse short channel effects; punch through; mobility degradation; velocity saturation[1].

2. Theoretical Background

2.1. Classification of the MOSFET Transistors

In Figure 1 is presented the perspective projection of MOSFET Transistor[2].

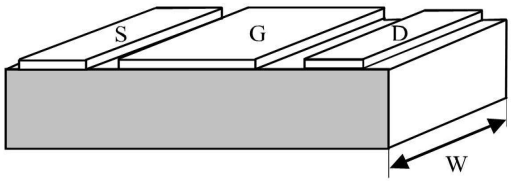

Figure 1. MOSFET Transistor (perspective projection) In Fig. 2, is shown a long-channel MOSFET Transistor (cross section)[2]

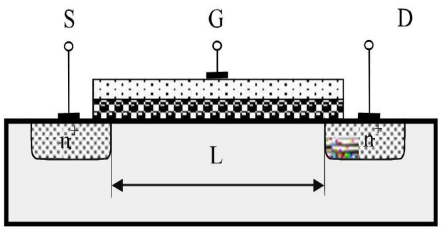

Figure 2. Long-channel MOSFET Transistor(cross section) If the channel length L >> sum of the depletion widths of the drain and the source, as shown on Figure 2, the MOSFET Transistor is classified as long-channel [1], [2]

Contrariwise, if L is comparable with the sum of the source and drain depletion widths, as presented on Figure 3 the MOSFET Transistor is classified as short-channel [1], [2].

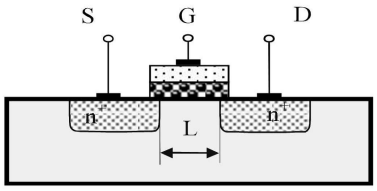

Figure 3. Short-channel MOSFET Transistor(cross section)

2.2. Basic Mathematical Equations [3]

a) In the triode area the equation (1) is valid [3]:

$$I_{D0} = \mu_n . C_{ox} . \frac{W}{L} . \left[\left(V_{GS} - V_{th0} \right) . V_{DS} - \frac{V_{DS}^2}{2} \right], \tag{1}$$

where [3],[1]: I_{D0} designates the value of the drain current, ignoring the effect of the channel length modulation; C_{ox} is the gate oxide capacitance per unit area; V_{th0} is the threshold voltage; μ_n is the field effect mobility of electron[1]; V_{DS} is the voltage drain-source; V_{GS} is the voltage gate-source.

b) In the saturation area [3]:

$$I_{D0} = \frac{\mu_n . C_{ox}}{2} . \frac{W}{L} . \left(V_{GS} - V_{th0} \right)^2 \tag{2}$$

The transconductance can be calculated by means of the relation (3)[3]:

$$g_m = \mu_n . C_{ox} . \frac{W}{L} . \left(V_{GS} - V_{th0} \right) = \sqrt{2 . \mu_n . C_{ox} . \frac{W}{L} . I_{D0}} \tag{3}$$

2.3. Short Channel Effects[3], [2]:

* Channel length modulation [3]

By channel length modulation the equations (1) and (2), concerning the drain current in triode area and in the saturation area, can be presented as follows[3]:

$$I_D = \left(1 + \lambda . V_{DS} \right) . I_{D0} \tag{4}$$

where λ is semi empirical constant.

* Threshold voltage roll off [2]
The threshold voltage of short-channel N - MOSFET Transistor is less than the corresponding threshold voltage of the long - channel MOSFET Transistor. It can be calculated by means of the relation [2]:

$$V_{th0\ short\ channel} = V_{th0\ \ long\ channel} - \Delta V_{th0}, \tag{5}$$

where:

$$\Delta V_{th0} = \frac{1}{C_{ox}} \cdot \sqrt{2.q.\varepsilon_{Si}.N_A\left|-2.\phi_f\right|} \cdot \frac{x_j}{2.L} \cdot \left[\left(\sqrt{1+\frac{2.x_{dS}}{x_j}} - 1\right) + \right. \tag{6}$$

$$\left. + \left(\sqrt{1+\frac{2.x_{dD}}{x_j}} - 1\right)\right] [2]$$

Here [2]: x_{dS} is the depth of the depletion region at source; x_{dD} is the depth of the depletion region at drain; N_A is the substrate doping density; ϕ_f is the substrate Fermi potential; ε_{Si} is the dielectric constant of silicon; q is the electron charge; C_{ox} is the gate oxide capacitance per unit area; x_j is the junction depth. The depletion regions are detailed presented on Figure 4[2]:

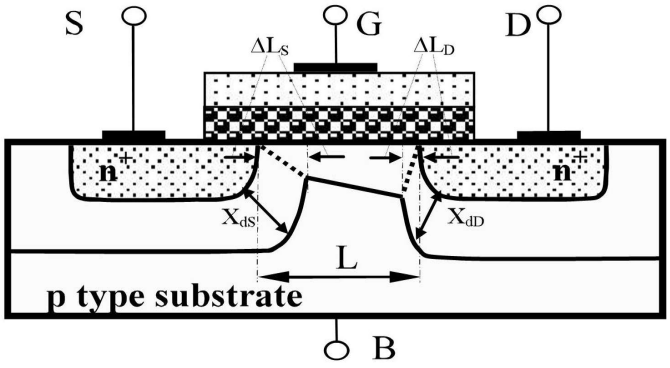

Figure 4. MOSFET Transistor structure (cross section)

* Punch through[3]
When the depletion region at source X_{dS} and the depletion region at drain X_{dD} merge there is a punch through. The drain current cannot be driven by gate voltage.

* Velocity saturation[3]
In order to realize ever smaller in size devices modern technologies have been applied. In this case high-field effects must be taken into account. In this analysis essential is the effect of velocity saturation. In silicon the electron drift cease to depend from the applied electric field at value approximately 106 V/m and saturates at a value of approx. 10^5 m/s. The result, obtained from the expression: $\frac{V_{GS}-V_{th0}}{L}$ plays an important role by the short-channel effects. In case, that $\frac{V_{GS}-V_{th0}}{L}$ approaches E_{sat}, where E_{sat} is typical approximately $4.10^6 V/m$, I_D is not more dependent from L.

$$I_D = \frac{\mu_n.C_{ox}}{2}.W.\left(V_{GS}-V_{th0}\right).E_{sat}\ [3] \tag{7}$$

The velocity saturation leads to restriction of the value of the transconductance: $\omega_T \approx \frac{3}{4}.\frac{\mu_n.E_{sat}}{L}$ [3] (8)

$$g_m = \mu_n . C_{ox} . \frac{W}{2} . E_{sat} \text{ [3]} \quad (8)$$

For its part the transit frequency can be expressed as follows:

$$\omega_T \approx \frac{3}{4} . \frac{\mu_n . E_{sat}}{L} \text{ [3]} \quad (9)$$

The reverse short-channel effects are related to the doping profile of the analyzed MOSFET device[3]

* Narrow channel width effects[2]

Considerations about the channel width: the analysis is similar to the analysis, concerning the channel length. If the channel width W is comparable with the maximum depletion regions thickness into the substrate (x_{dm}) , the MOSFET Transistor can be classified as narrow-channel. The narrow channel effect leads to increase of the threshold voltage [2]:

$$V_{th0\ narrow\ \ channel} = V_{th0\ long\ channel} + \Delta V_{th0} \quad (10)$$

In case that the shape of the depletion regions edges are modeled by means of quarter circular arcs the following expression is valid [2]:

$$\Delta V_{th0} = \frac{1}{C_{ox}} . \sqrt{2.q.\varepsilon_{Si} . N_A \left| -2.\phi_f \right|} . \frac{\pi . x_{dm}}{2.W} \quad (11)$$

* Mobility degradation[3]
The increase of the gate potential leads to decrease of the mobility of the charge carriers. This effect can be quantitative evaluated by means of the normal field mobility degradation factor θ. It has a typical value in the range: $(0{,}1 \div 1)\, V^{-1}$ and is inversely proportional to the gate oxide thickness. In order to obtain the actual value of the drain current I_D the calculated value must be multiplied by [3]:

$$\frac{1}{1 + \theta . \left(V_{GS} - V_{th0} \right)} \quad (12)$$

3. PSPICE Models of the Analyzed Circuits

In traditionally courses the focus of the analysis of the MOSFET devices is aimed toward the basic characteristics. In this paper special attention is turned on the short channel effects in MOSFET Transistors.

The circuit, which has been used in the presented paper for AC analysis, is shown on the Figure bellow.

The circuit for analysis of mobility degradation and the dependence on the oxide thickness is displayed on Fig.6. In order to study the roll-off effect the circuit, presented on Figure 6, is used.

The PSPICE models of the transistors in these circuits are based on the Level 3 PSPICE parameters, given in [3]. The narrow gate width effects have been investigated by means of the both circuits (shown on Figure 5 and Figure 6).

The channel length modulation has been examined using the PSPICE MOSFET parameters Level 2, presented in [4].

As it can be seen from the analysis setup conditions concerning the circuit, presented on Figure 6, DC nested sweep has been activated. The gate voltage changes in the range: 0V ÷ 5V while the bulk voltage vary from 0V to 8V by step of increment 2V.

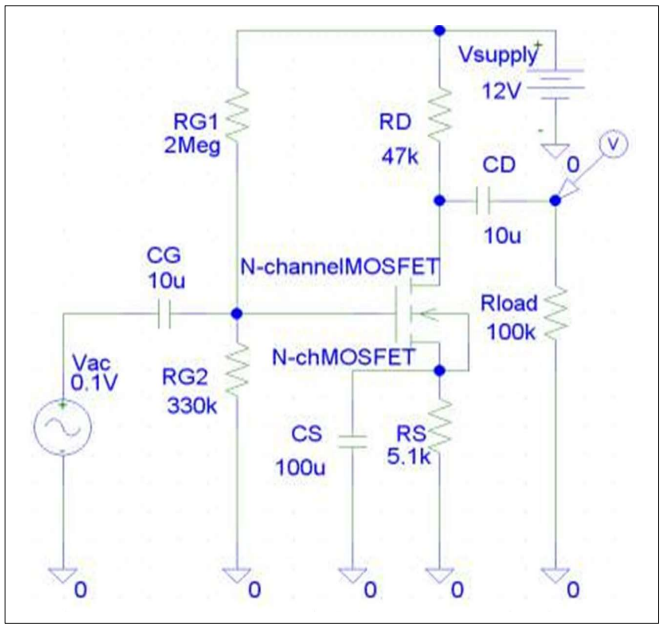

Figure 5.PSPICE model for AC analysis

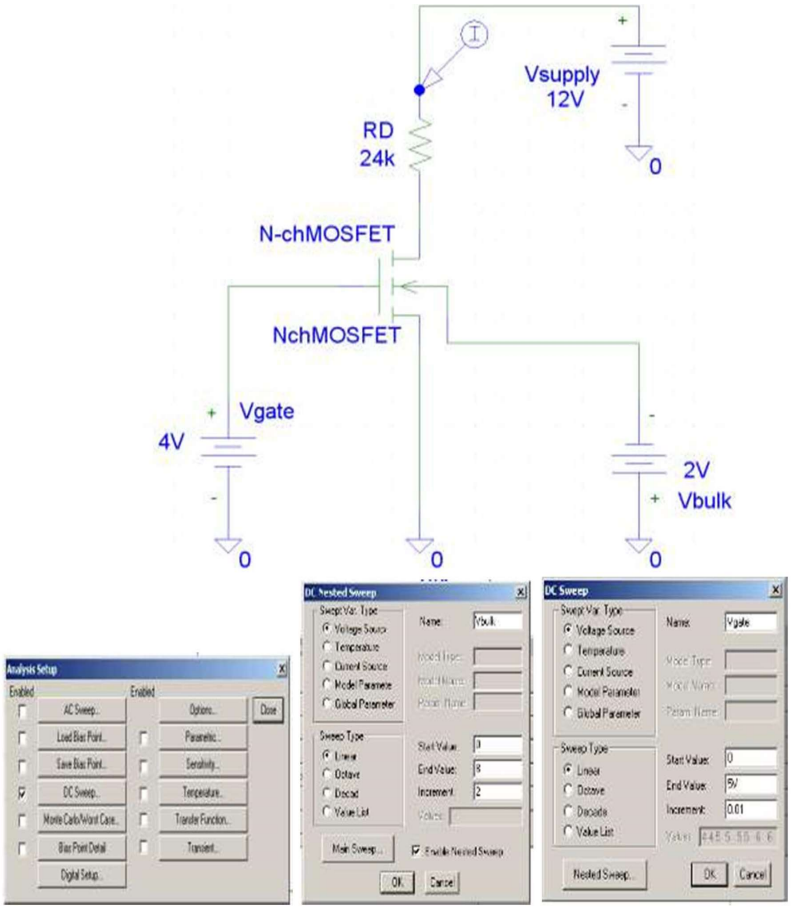

Figure 6. PSPICE models for studying roll-off effect

4. Imulation Results and Analyzes

4.1. Mobility Degradation

The simulation experiments, concerning the AC analysis, have been done by mobility degradation factor θ (THETA) = $2{,}3.10^{-1}$, as given in [3]. The results are presented on Figure 7.

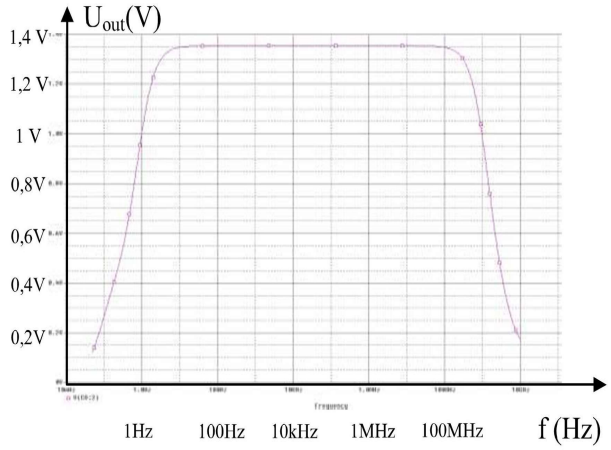

Figure 7. AC analysis by θ (THETA) = $2, 3.10^{-1}$

The circuit, displayed on Figure 5, has been used by the simulation. Changing the value from θ = $2{,}3.10^{-1}$ to θ = 1 leads to consequent change in the AC characteristic. This is displayed on Figure 8.

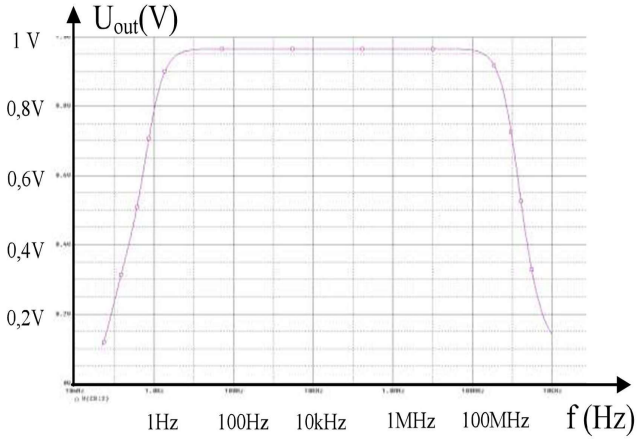

Figure 8. AC analysis by θ (THETA) = 1

As expected, taking into account the analytical expression (12), from the Figures above, becomes obvious that the output voltage is inverse proportional to the value of θ.

By the both simulations the value of the oxide thickness is $9, 5.10^{-9}$.

4.2. Influence of the Oxide Thickness

In order to establish qualitative relationship between this thickness and the AC parameters of the MOSFET amplifier another simulation has been performed.

Changing the oxide thickness from $9{,}5.\ 10^{-9}$ to 3.10^{-9} the following results, displayed on Figure 9, are obtained.

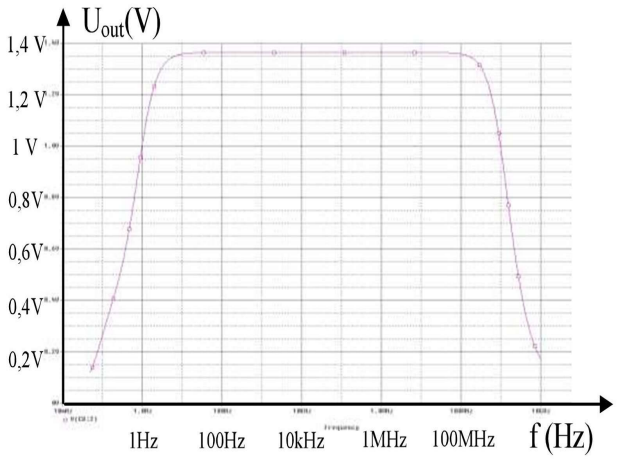

Figure 9. AC analysis by oxide thickness 3.10^{-9}, = 2, 3.10^{-1}

All simulations up to here have been done by: L = 2μm and W = 16 μm.

4.3. Narrow Channel Width Effects

In order to analyze the narrow gate width effects the value of W has been reduced to 8m. The value of L remains 2μm, θ = 2, 3. 10^{-1}, the oxide thickness is $9{,}5.10^{-9}$. Taking into account the equations: (1), (2), (3) decrease of the output voltage is expected. This is presented on Figure 10.

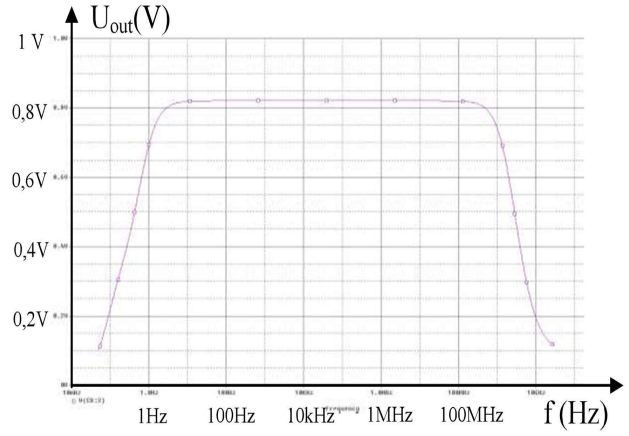

Figure 10. AC analysis by W = 8 μm

The graphical results, shown on Figure 10, confirm these expectations.

4.4. Roll off Effects

The investigations, concerning the roll-off effects, have been performed by means of the circuit, presented on Figure 6. The simulation results, done by L = 2 μm, W = 16μm, are displayed on the Figure bellow.

Figure 11.Characteristic I_D - V_{GATE} by L = 2 μm, W = 16 μm The change of the bulk voltage toward more negative values leads to subsequent translation of the characteristic I_D - U_{GATE} to the right, as it becomes obvious from Figure 11.

4.4.1. Narrow Channel Width Effects

According to expressions (11),(10) the reduction of width W to 8μm leads analytically to increase of the threshold voltage. By initial conditions L= 2 μm W = 8 μm simulations have been done. The results are presented on Figure 12.

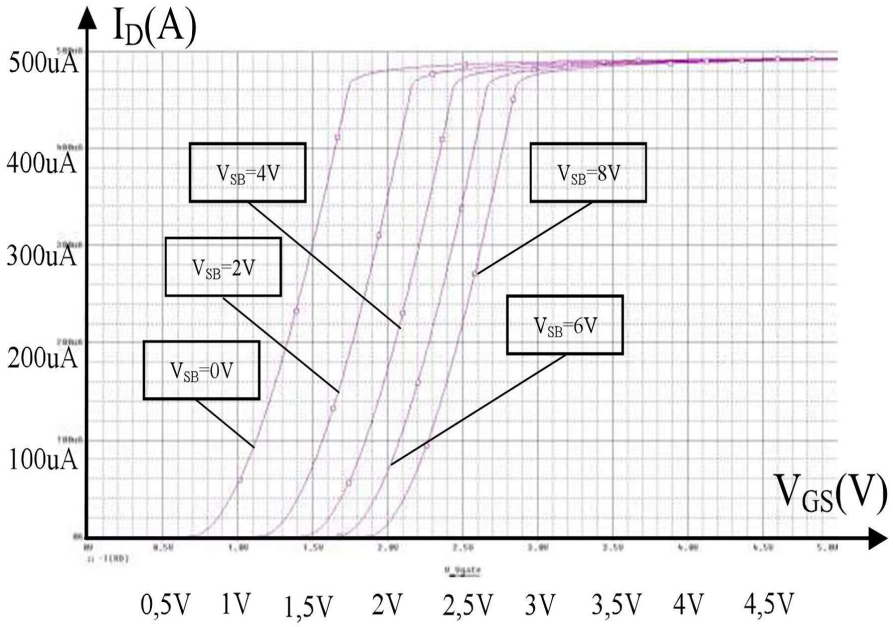

Figure 11.Characteristic I_D - V_{GATE} by $L = 2$ μm, $W = 16$ μm

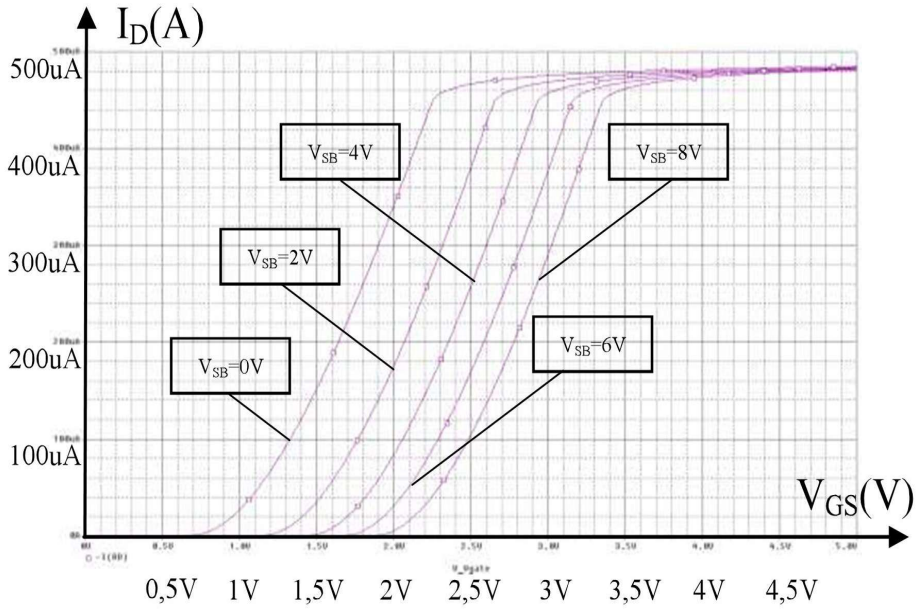

Figure 12. Characteristic I_D - V_{GS} by L = 2 μm, W = 8 μm

Comparing the characteristics from Figure 11 and Figure 12 the increase of the threshold voltage can distinctly be seen.

4.4.2. Short Channel Effects

While the width W reduction leads to increase of the threshold voltage, according to expressions (6) and (5), the supposedly decrease of the channel length L should cause increase of ΔV_{th0} and subsequent decrease of the threshold voltage $V_{th0\ short\ channel}$. Simulations using PSPICE model attributes L = 0,5μm, W = 8μm have been done. The obtained results are presented on Figure 13.

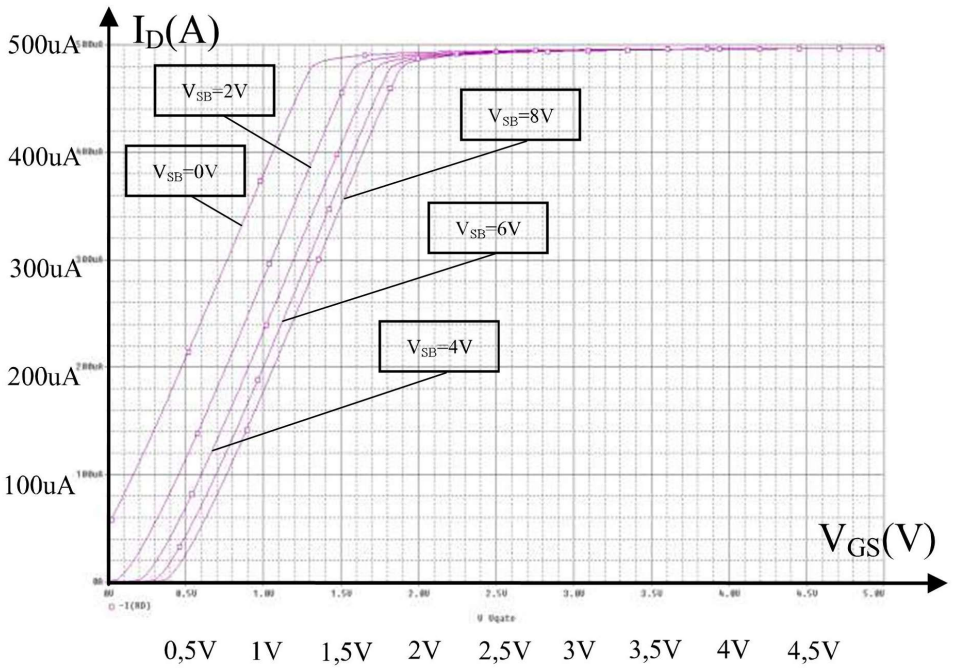

Figure 13. Characteristic ID - VGS by L = 0,5 μm, W = 8 μm

The translations of the characteristics to the left, compared to the characteristics, displayed on Figure 12, confirm the expected effect of decrease of the threshold voltage.

4.5. Channel Length Modulation

By the simulations the PSPICE model, proposed in [4], has been used. The values of V_{SB}, L and W have been set to: V_{SB} = 2V, L = 2 μm , W = 16 μm .

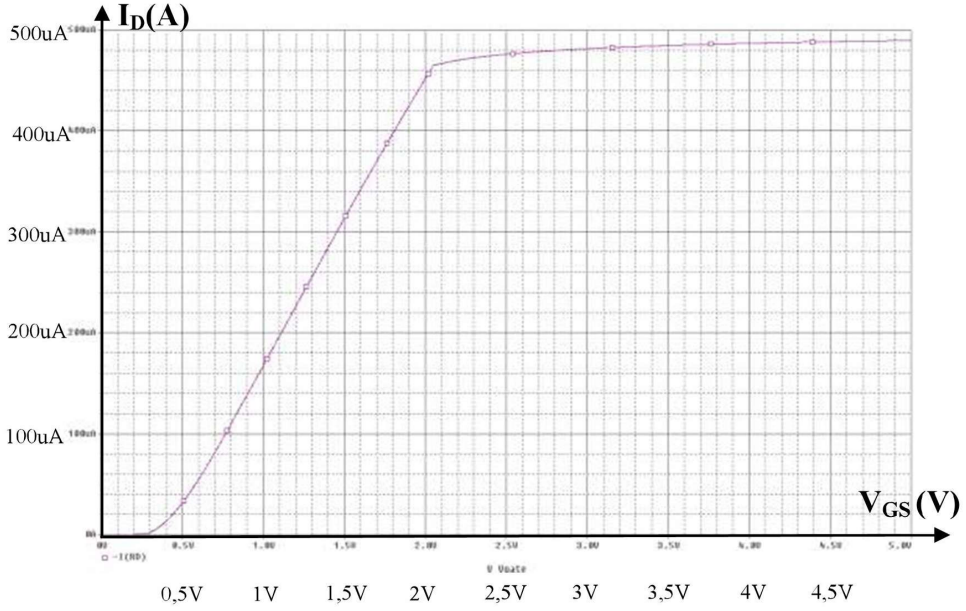

Figure 14. Characteristic ID - VGS by $\lambda = 3{,}903.10^{-2}$

The graphical results, shown above, concern the PSPICE model parameter values, given in [4]. The value of λ (LAMBDA), given there, is $3{,}903.10^{-2}$. In order to study the influence of the value of parameter upon the drain current, which analytically is described by means of expression (4), another value of λ has been inserted in the PSPICE model of the MOSFET Transistor. In this case λ has been set to value of 1.10^{-2}.

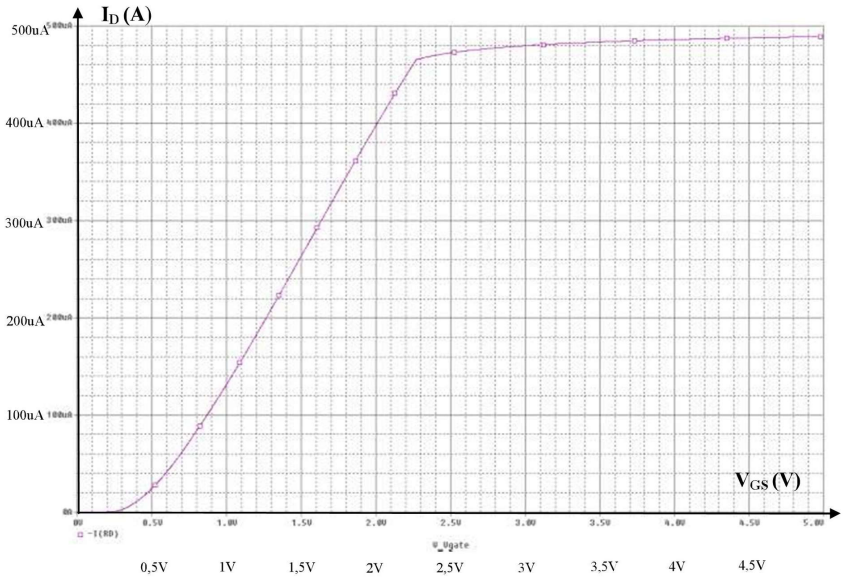

Figure15. Characteristic ID - VGS by $\lambda = 1.10^{-2}$

An essential change in the slope of the characteristic ID - VGS, displayed on Figure 15, in comparison with the slope of the characteristic I_D - V_{GS}, presented on Figure 14, has been found out. This fact is in accordance with the analytical expression, concerning I_D, given in (4).

5. Conclusion

In this paper the short channel effects in MOSFET devices are discussed. The goal of the paper is to present a set of simulation experiments, in order a detailed examination of these effects to be performed.

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