Measuring the Efficiency of Gallium Transistors for Buck Converters

Zoran Zivanovic[1] and Vladimir Smiljakovic[2]
IMTEL KOMUNIKACIJE AD
Bul. Mihajla Pupina165b
11070 Belgrade
Serbia
{zoki@insimtel.com} {smiljac@insimtel.com}

ABSTRACT: *This paper reports the use of Gallium transistors for creating models of buck converters. With the help of the functional block diagrams, we have described the operating principles. To confirm and ensure the functioning of the created model we have developed pilot system that is experimented with various calculations. Our purpose is to prove the ability of the transistors to explain the benefits of silicon use.*

Keywords: Buck, Efficiency, eGaN, Figure of Merit, Synchronous

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1. Introduction

Rapid commercialization of switch mode power supplies was made possible by mass production of silicon power MOSFETs in the late seventies. Constant demand for more efficient power converters, with higher efficiency and smaller size, forced the power supply engineers to reduce losses and increase the switching frequency. After 30 years, silicon MOSFET development has approached its theoretical limits. In contrast, the production of the enhancement mode gallium nitride FETs started in 2009, and is less investigated in literature [1]-[5]. A major factor in eGaN FETs performance is die (Fig. 1) that minimizes parasitic elements and allows footprint that helps to make optimal layout design. Interleaved drain and source bars generate small loops with opposing current flow, resulting into magnetic field cancellation and smaller common source inductance.

The objective of this paper is to contribute to the analysis of eGaN FETs characteristics by measuring the efficiency and capturing the waveforms of the synchronous buck converter with eGaN FETs over a wide range of operating conditions.

The paper is organized as follows. In Section 2, synchronous buck converter basics are given. Two state of the art MOSFETs are compared with two eGaN FETS with the same voltage rating in section 3 with calculations of critical parameters and components using design equations. Experimental results of a synchronous buck converter with eGaN FETs are presented in section 4 to validate design. At the end, the conclusions are given in section 5.

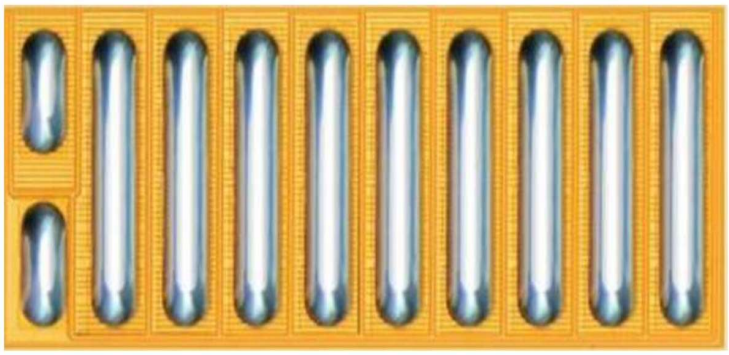

Figure 1. eGaN EPC2015C passivated die (size 4.6 x 1.6 mm)

2. Synchronous Buck Converter Basics

The synchronous buck converter is given in Figure 2.

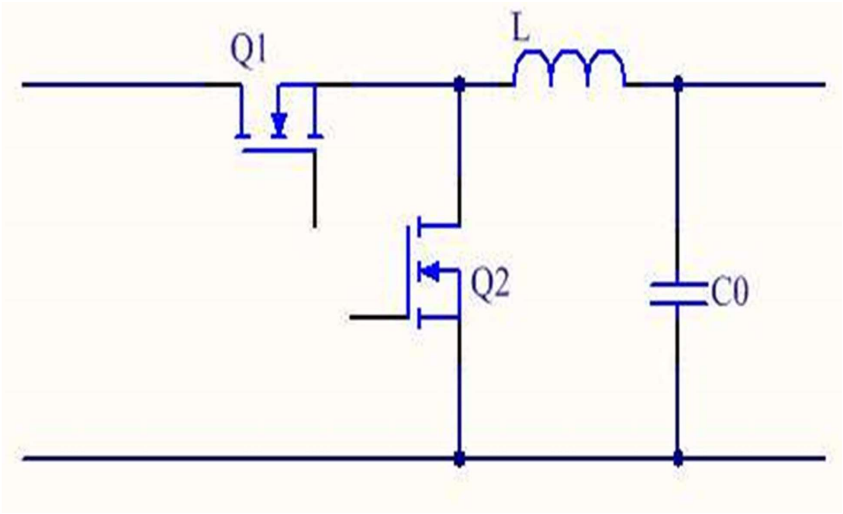

Figure 2. Synchronous buck converter

When the switch Q_1 is ON during T_{ON} the energy is transferred to the output as well as to the inductor L. The current flows through the switch Q_1 and the inductor. The difference of voltages between V_{IN} and V_{OUT} is applied to the inductor and the inductor and switch current I_{D1} rises linearly. During the OFF period of time, when the switch Q_1 is OFF, the inductor current continues to supply load current. The switch Q_2 is ON providing freewheeling path for the inductor current. The output voltage is applied to the inductor, so the inductor current decreases linearly (Figure 3).

The inductor current flows to the capacitor and the load. The capacitor CO acts as a reservoir and holds the output voltage nearly constant.

3. Design and Analysis

To design synchronous buck converter, we will start from the design specifications given in Table 1.

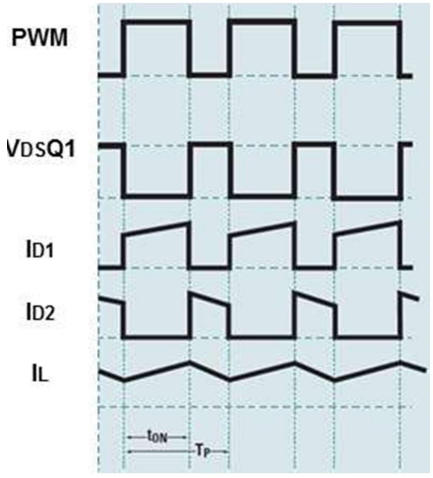

Figure 3. Synchronous buck converter waveforms

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3. Design and Analysis

To design synchronous buck converter we will start from the design specifications given in Table 1.

		Min	Typ	Max	
Input voltage	V_{IN}	8	12	18	V
Output voltage	V_O		5		V
Output current	I_O	0.1	7		A
Output current limit	I_{OCL}		8.4		A
Full load efficiency	η		> 90		%
Switching frequency	f_{SW}		440		KHz

Table 1. Design Specifications

In order to dampen sub-harmonic oscillation, the minimum inductor value should be calculated as

$$L = \frac{V_O}{0.3 f_{SW} I_O} \tag{1}$$

The maximum and minimum duty cycle can be calculated as

$$D_{MAX} = \frac{V_O}{V_{INMIN}} \tag{2}$$

$$D_{MIN} = \frac{V_O}{V_{INMAX}} \tag{3}$$

The peak to peak inductor current is

$$\Delta I = \frac{V_{INM} - V_O}{L} \frac{D_{MIN}}{f_{SW}} \tag{4}$$

Knowing that the peak inductor current is

$$I_{pk} = I_O + \frac{\Delta I}{2} \tag{5}$$

The output capacitor must be large enough to limit the voltage overshoots and undershoots during the load change transients. The minimum value of output capacitor is

$$C_{O\min} = \frac{LI_{step}^2}{2\Delta V_O D_{MAX}(V_{INM} - V_O)} \tag{6}$$

The power switches must be chosen with voltage rating to withstand the maximum input voltage and also they must be capable of delivering the load current. Knowing that, our choice is two MOSFETs (IPC50N04S5L-5R5 and IPZ40N04S5L-7R4) and two eGaNs (EPC2014C and EPC2015C). We will use figure of merit (FOM) expressed by the equation

$$FOM = \left(Q_{GD} + Q_{GS}\right) R_{DS} \tag{7}$$

as a selection criteria. Results are given in Table I. Although both MOSFETs are state of the art power switches, the eGaN FETs are better choice because of superior switching characteristics and zero reverse recovery time.

	Q_{GD}	Q_{GS}	R_{DS}	FOM	Q_{rr}
IPC50N04S5L	3.6nC	2.7nC	5.7mΩ	35.91	22ns
IPZ40N04S5L	3.0nC	2.0nC	7.9mΩ	39.5	26ns
EPC2014C	0.3nC	0.7nC	12mΩ	12	0ns
EPC2015C	1.2nC	2.7nC	3.2mΩ	12.48	0ns

Table 2. Power Switch Characteristics

The high side FET losses can be calculated as

$$P_{DQ1} = I_O^2 R_{DS} D_{MAX} + \frac{1}{2} V_{IN}(t_r + t_f) I_O f_{SW} \tag{8}$$

The losses in the low side FET can be expressed as

$$P_{DQ2} = I_O^2 R_{DS}(1 - D_{MIN}) + I_O(t_{dr} + t_{df}) f_{SW} V_D + Q_{rr} f_{SW} V_{IN} \tag{9}$$

Calculated values are given in Table 3.

Inductance calculated	L	5.4	µH
Inductance adopted	L	6.8	µH
Max duty cycle	D_{MAX}	0.625	
Min duty cycle	D_{MIN}	0.277	
Peak to peak current	ΔI	1.2	A
Peak current	I_{pk}	7.6	A
Min capacitance	C_{Omin}	290	µF

Table 3. Calculated Values

We will also adjust passive components around the error amplifier in order to have 25kHz loop abndwidth with 60^0 phase margin.

4. Realization

The synchronous buck converter has been realized on a four layer FR-4 substrate, with a thickness of 1.6mm and 50µm copper on outer layers and 35µm on inner layers. The size of the PCB is 50x42 mm. For the high-side and low-side switches we have used eGaN FETs EPC2015C. The eGaN FETs have a maximum gate voltage of +6V. The buck controller LM5141, require a logic-level FETs, so it is a great choice for this design. The output filter is made of four pcs of multilayer ceramic capacitors 47 µF, 10V, X7R, to reduce high frequency noise and two 100µF, 10V tantalum capacitors for energy storage.

Using lab power supply and electronic load, we have recorded the waveforms of interest and measured efficiency at various loads and input voltages.

Drain voltage of the high side GaN FET is given in Figure 4. His gate voltage is given in Figure 5. Turn-on waveform of highside GaN FET with parasitic 125 MHz ringing is given in Figure 6. Drain voltage of the low-side side GaN FET is given in Figure 7 and his gate voltage is given in Figure 8. The 125 MHz ringing on the drain of the low-side GaN FET at turn-off is given in Figure 9. Measured efficiency of the converter is given in Figure 10.

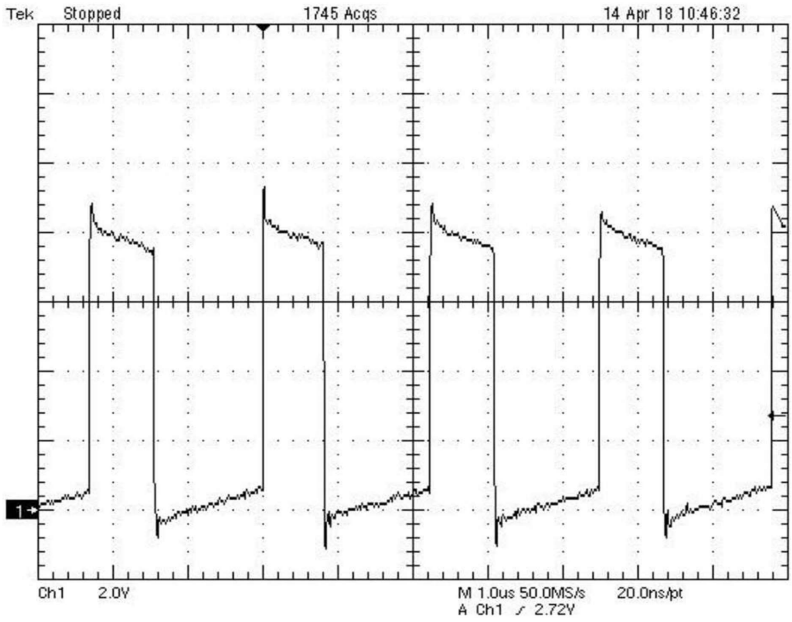

Figure 4. Drain voltage of high-side GaN FET

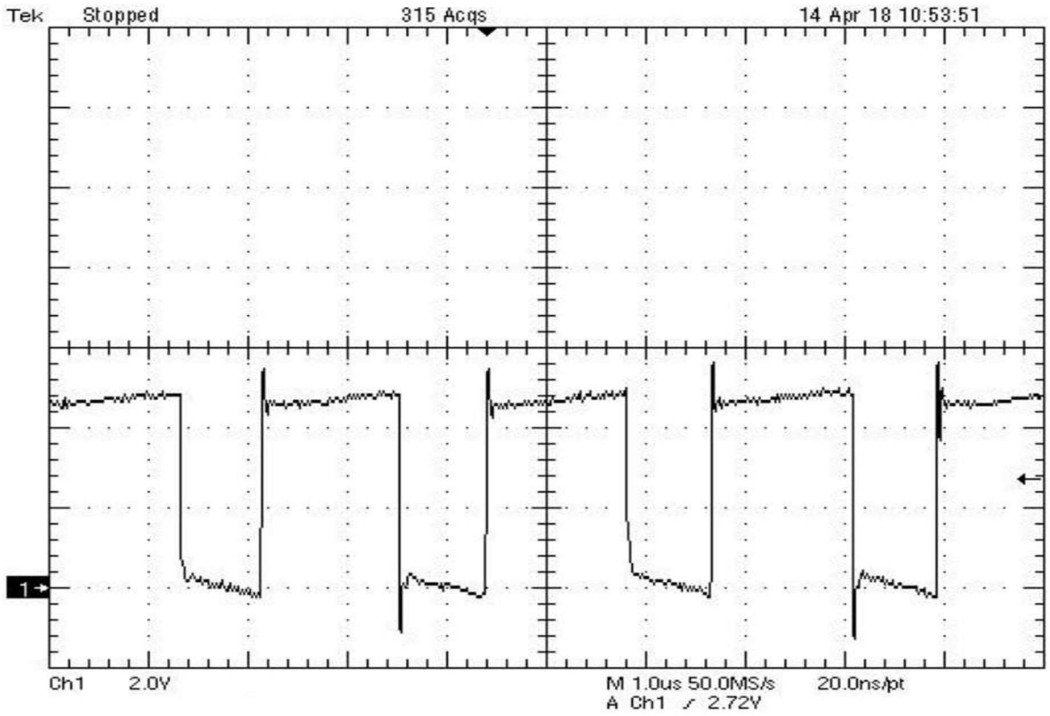

Figure 5. Gate voltage of high-side GaN FET

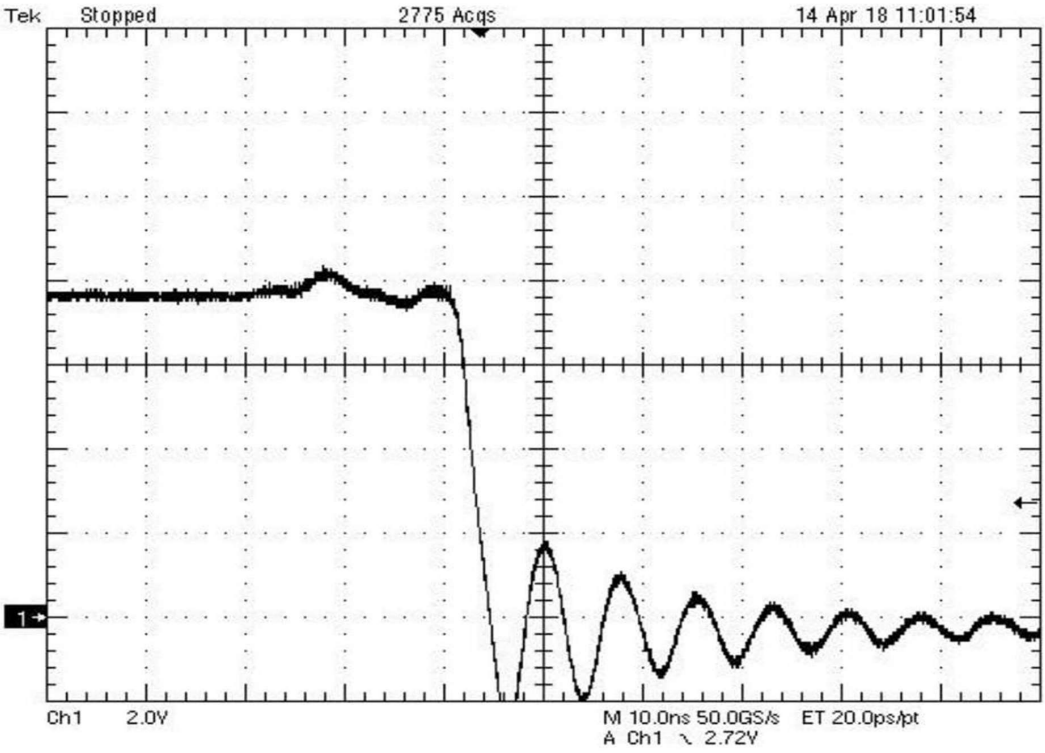

Figure 6. Turn-on waveform of high-side GaN FET

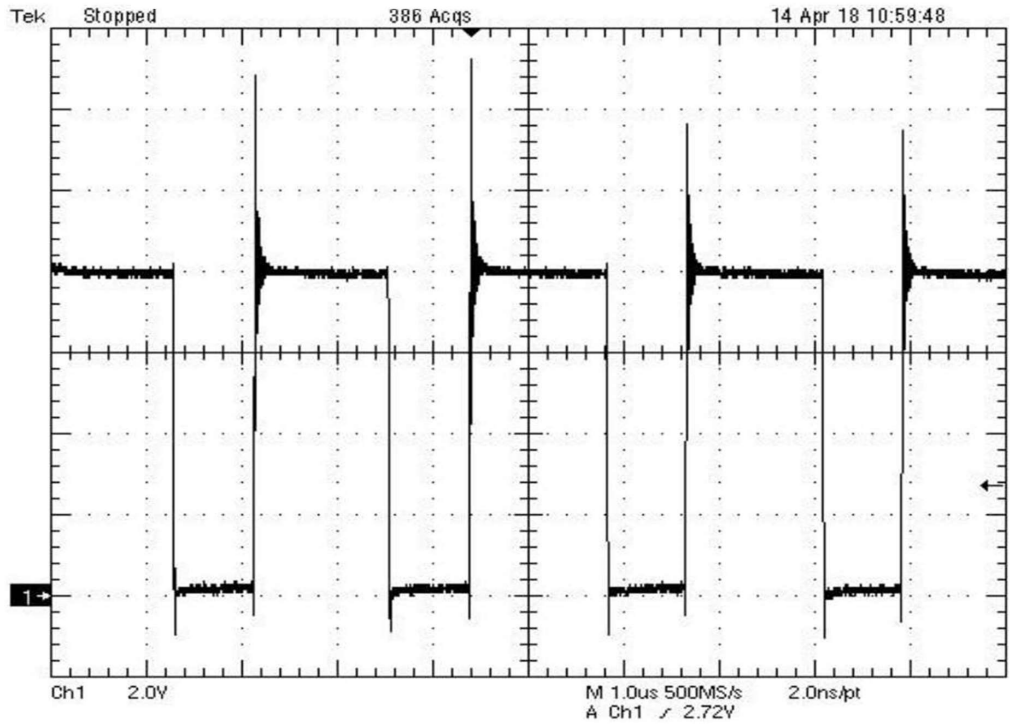

Figure 7. Drain voltage of low-side GaN FET

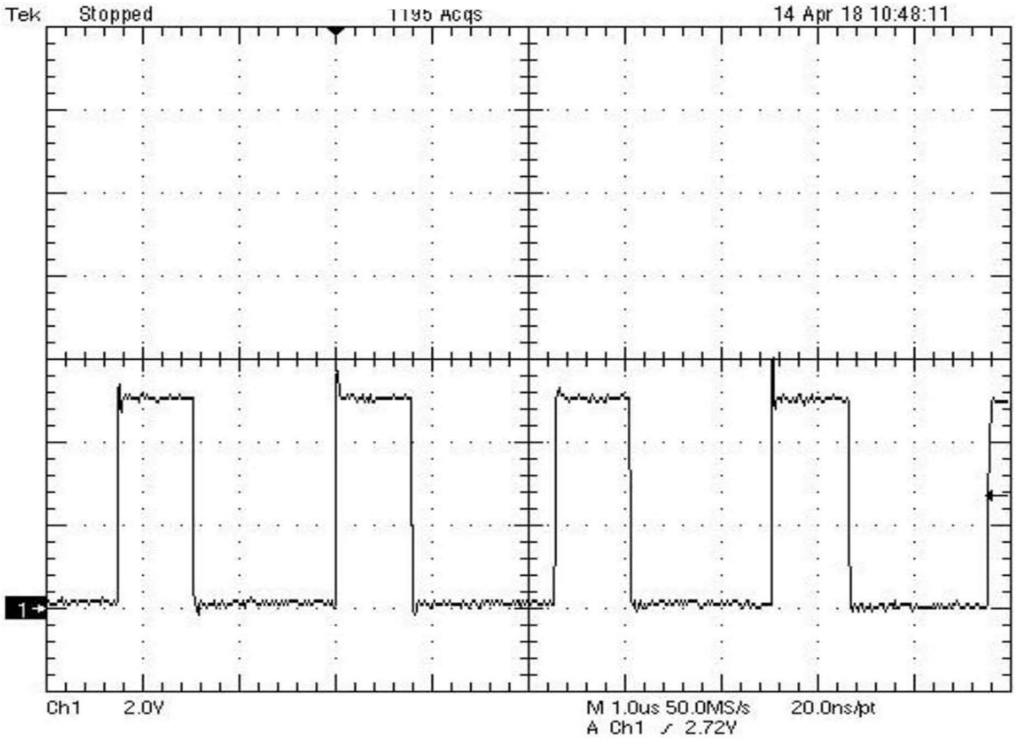

Figure 8. Gate voltage of low-side GaN FET

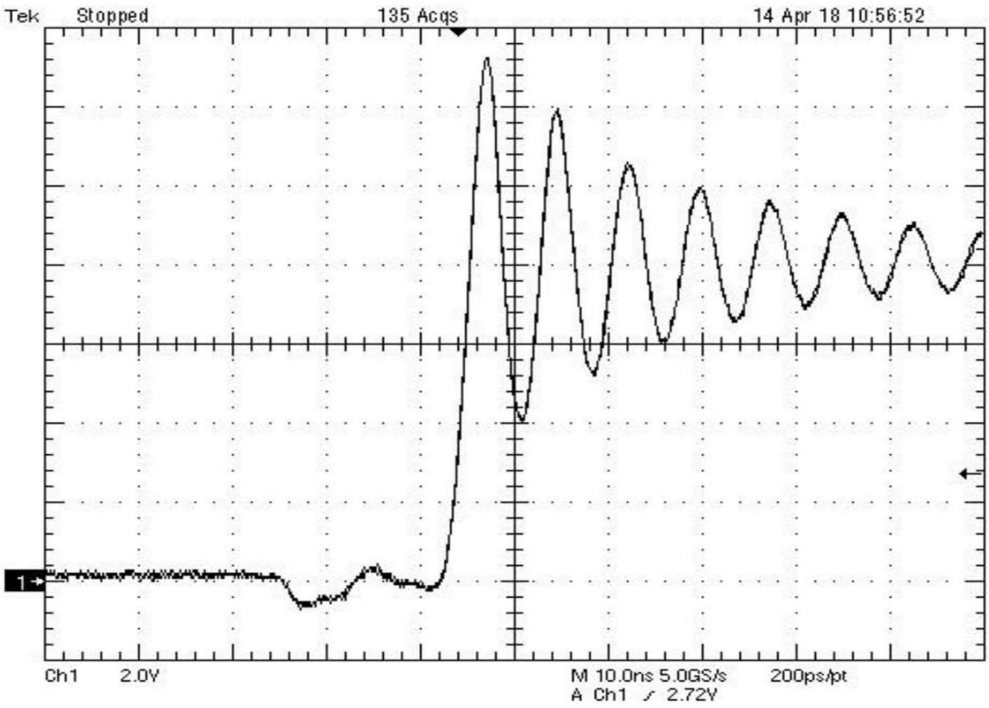

Figure 9. The ringing on the drain of low-side GaN FET at turn-off

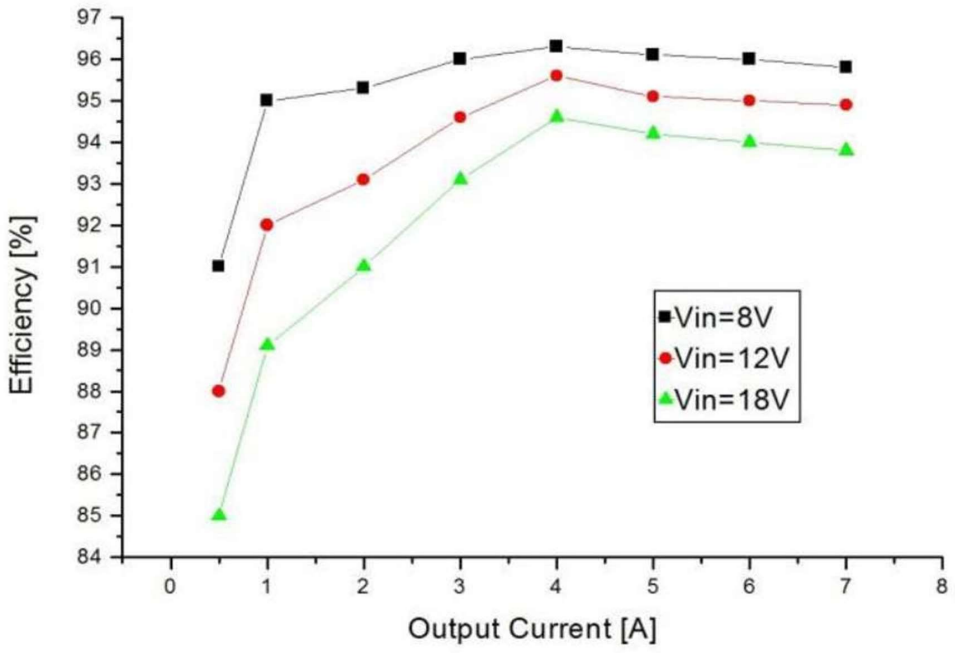

Figure 10. Measured efficiency vs. output current

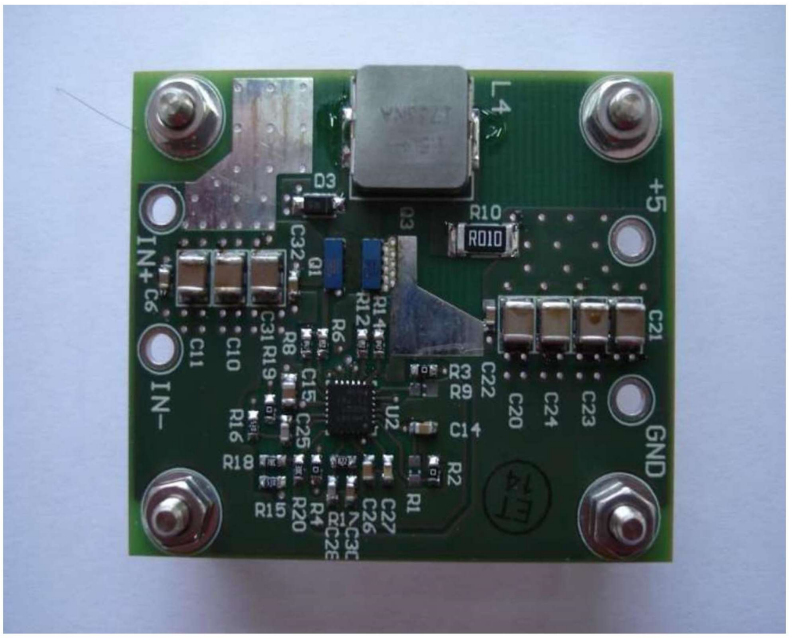

Figure 11. The converter prototype

Figure 12. Experimental setup in the lab

5. Conclusion

In this paper the design and realization of a synchronous buck converter with GaN FETs is presented. Calculations and experimental results are presented. The prototype was built and tested. The results verified that the efficiency can go as high as 96%.

Acknowledgement

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