

Silicon Carbon Diodes for Power Converter Design

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ABSTRACT: *With the help of Nitride transistors and Silicon Carbide diodes, the design for the interleaved power factor correlation converter is generated in this paper. The modified schema and its system of operation for the converter are explained. To test the validity of the design, simple experimentation is performed, which shows interesting results. These results support the basic principles we have used for the design and prove the performance of the converters. The aim thus is to prove the power factor generators' performance in high-power use.*

Keywords: Boost, Efficiency, GaN, Interleaved, PFC, SiC

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1. Introduction

Most off-line power supplies have a front end section made by a rectification bridge and a filter capacitor. Such power supply draws a current pulse during a small fraction of the each half-cycle duration. Pulsed current waveform produce non efficient RMS currents affecting the real power available from the mains [1]. In order to utilize the full line power and to reduce line current harmonics Power Factor Correction (PFC) circuits are required. The most popular PFC converter is a boost converter (Fig. 1). Mostly because the boost converter can have continuous input current that can be modulated with average current mode control to force the input current to track changes in the line voltage.

2. Interleaved PFC Converter

The two phase interleaved PFC converter shown in Figure 2 is practically made from two boost converters (phases) operating at the same frequency but 180° out of phase [2, 3].

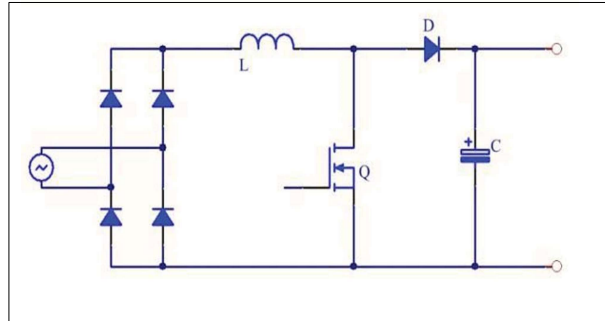


Figure 1. PFC converter

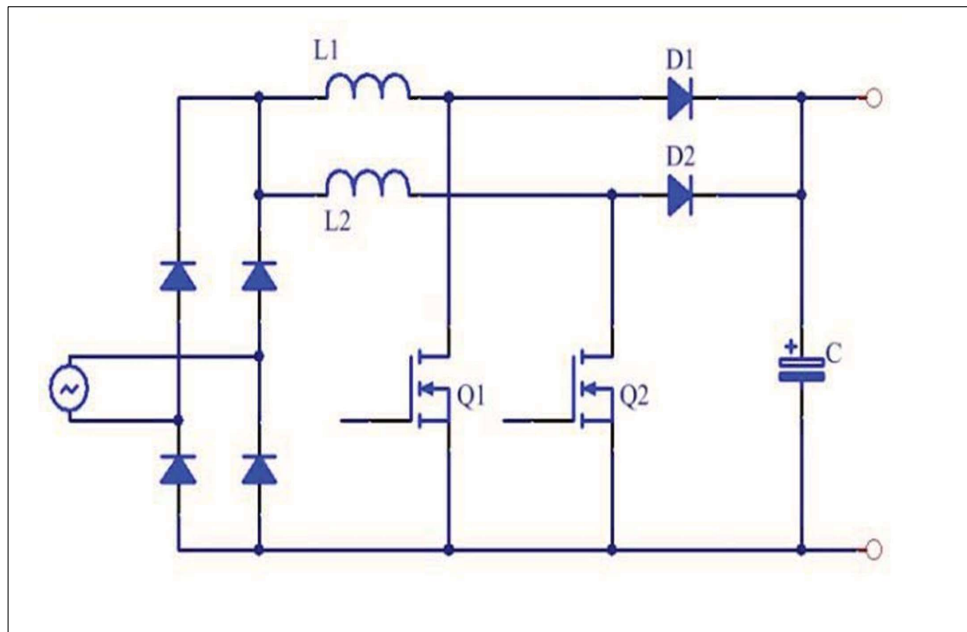


Figure 2. Interleaved PFC converter

The input current is the sum of the two inductor currents.

These currents are out of phase and tend to cancel each other, reducing the input ripple current caused by the boost inductors. The output bulk capacitor current is the sum of the two diode currents reduced by the load current. As a result of interleaving its RMS value is reduced and the size of the bulk capacitor is also reduced. By splitting the current into two paths, the conduction losses of power switches Q_1 and Q_2 and inductors L_1 and L_2 are reduced. The inductors magnetic volume is lower, because the energy storage requirement of the two interleaved inductors is two times smaller relative to the single inductor. The performances are improved at the cost of additional power switches, inductors and output diodes.

3. Design and Analysis

To design 1200W interleaved PFC converter we will start from the design specifications given in Table 1.

Converters duty cycle at the peak at low line operation is given by

$$D = \frac{V_{OUT} - V_{IN_MIN} * \sqrt{2}}{V_{OUT}}$$

		<i>Min</i>	<i>Typ</i>	<i>Max</i>
Input voltage (AC)	V_{IN}	173	220	265 V
Output voltage	V_O		400	V
Output current	I_O		3	A
Output current limit	I_{OCL}		3.3	A
Full load efficiency	η	96		%
Switching frequency	f_{SW}		100	kHz

Table 1. Design Specifications

Ripple current cancelation – ratio of input current to inductor ripple current at the peak at low line operation is

$$K = \frac{\Delta I_{IN}}{\Delta I_{L1}} = \frac{1 - 2 * D}{1 - D}$$

Inductor ripple current at the peak at low line operation can be calculated as

$$\Delta I_L = \frac{P_{OUT} \sqrt{2} * 0.3}{V_{IN_MIN} * \eta * K}$$

Minimum inductance of the boost inductors is

$$L_{1_MIN} = L_{2_MIN} = \frac{V_{IN_MIN} * \sqrt{2} * D}{\Delta I_L * f_{SW}}$$

Peak current of FETs and boost diodes is

$$I_{PK} = \left(\frac{P_{OUT} * \sqrt{2}}{2 V_{IN_MIN} * \eta} + \frac{\Delta I_L}{2} \right) * 1.2$$

RMS current of FETs is determined by

$$I_{RMS} = \frac{P_{OUT}}{2 * \eta * V_{IN_MIN} * \sqrt{2}} * \sqrt{2 - \frac{16 * V_{IN_MIN} * \sqrt{2}}{3 * \pi * V_{OUT}}}$$

Diodes average current is determined by

$$I_D = \frac{P_{OUT}}{2 * V_{OUT}}$$

Calculated values of the basic parameters of the each phase are given in Table 2.

		Max	Typ	Min	
Duty cycle	D			0.37	
Inductor ripple current	I_{PP}	7.88			A
Inductor RMS current	I_{LRMS}	4.23			A
Inductance	L			120	μH
FET RMS current	I_{RMS}	2.58			A
FET peak current	I_{PK}	11.12			A
Diode average current	I_{DAVG}	1.53			A
Diode peak current	I_{DPK}	11.12			A

Table 2. Basic Parameters of the each Phase

As a power switch we will choose between a 650V MOSFET IPW65R095C7 and GaN FET TPH3205WSB [4] whose characteristics are given in Table 3. GaN FET obviously has a better figure of merit (FOM) defined as

$$FOM = (Q_{GD} + Q_{GS}) * R_{DS}$$

The reverse recovery charge causes the boost diode to look

	Q_{GD}	Q_{GS}	C_{OSS}	R_{DS}	FOM
IPW65R095C7	15nC	12nC	33pF	84m Ω	2268
TPH3205WSB	6nC	10nC	135pF	49m Ω	784

Table 3. Power Switch Characteristics

like a short to the FET until the charge is cleared from the diode. This is a large source of switching loss in the PFC preconverter. Those losses are dependent on the peak operating current and diode temperature. A silicon carbide diode C3D08065I [5] is chosen because it has no reverse recovery charge and therefore zero reverse recovery losses.

The output capacitor is selected based on holdup requirements and can be calculated as

$$C_{OUT} \geq \frac{2 * P_{OUT}}{f_{LINE}[(V_{OUT})^2 - (0.65 * V_{OUT})^2]}$$

4. Realization

The interleaved PFC converter has been realized on two layer FR-4 substrate, with a thickness of 1.6mm and 70 μm copper with footprint 165 x 140mm. The boost inductors are wound on two stacked iron powder toroids. Low side driver UCC27511 is used. The output capacitor is made of three 270 μF electrolytic capacitors. Using isolation mains transformer and high power resistive load we have measured efficiency, power factor and also recorded the waveforms at the point of interest. Efficiency is over 98%, for 20 to 100% of the output power (Figure 3). The power factor is presented in Figure 4. Rectified line voltage and drain voltages are given in Figure 5. and Figure 6. Gate and drain voltage of the GaN FET are given in Figure 7. Input line current with the respect to the line voltage is given in Figure 8. Limited inrush current is recorded in Figure 9. Output line ripple is given in Figure 10. Output voltage startup into full load is given in Figure 11. The converter prototype with top heatsink removed is presented in Figure 12.

Finally, the experimental setup in the lab is given in Figure 13.

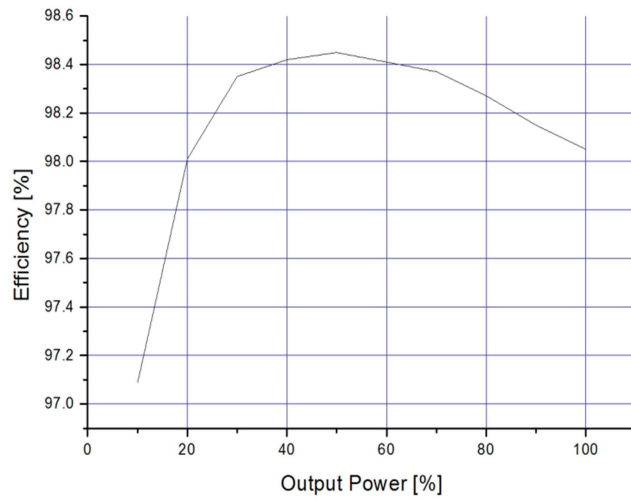


Figure 3. Efficiency at 220V input

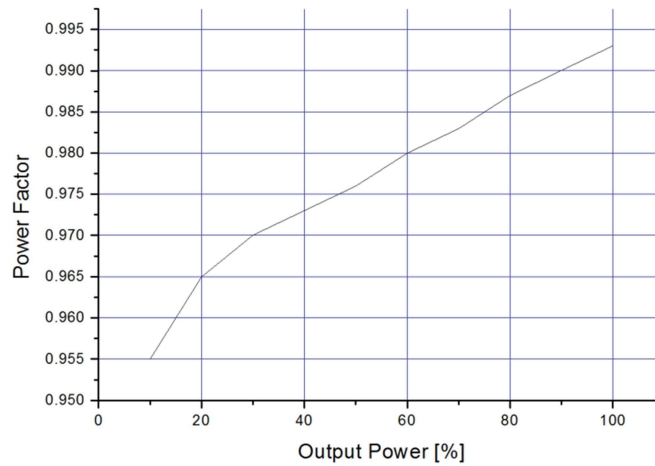


Figure 4. Power factor

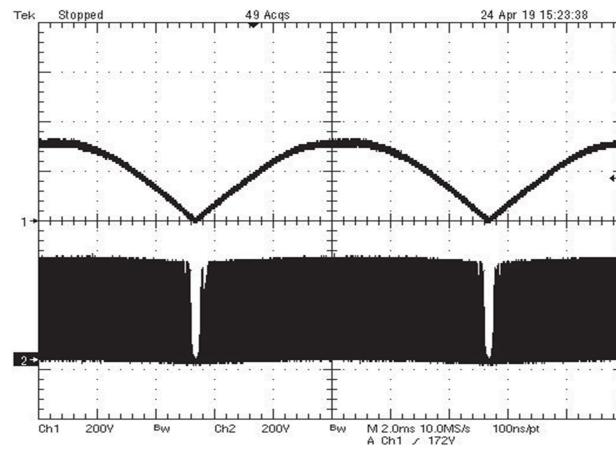


Figure 5. Rectified line voltage and drain voltage

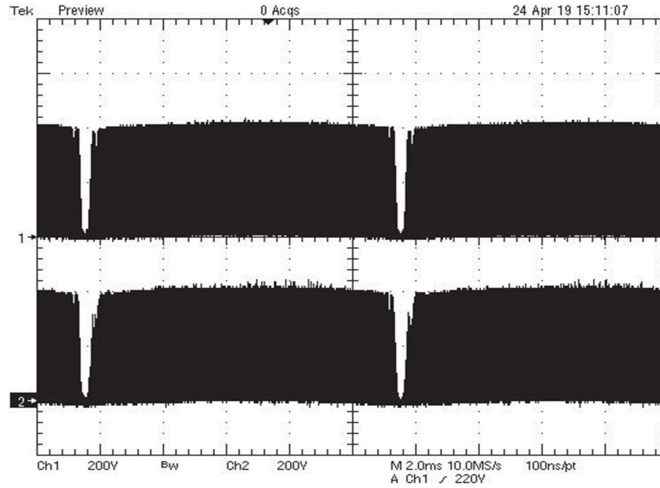


Figure 6. Drain voltage simetry

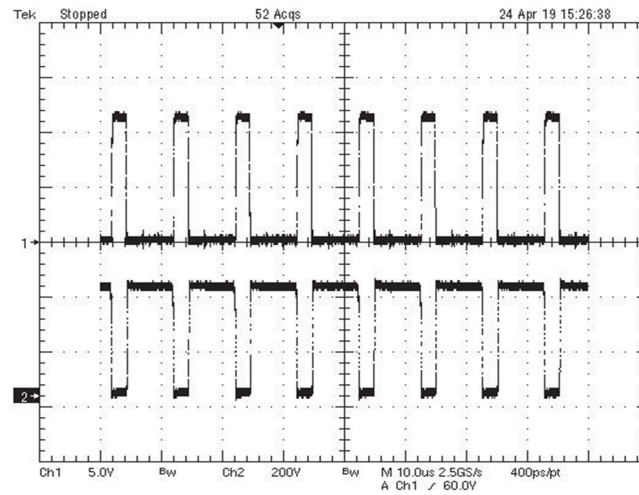


Figure 7. Gate and drain voltage

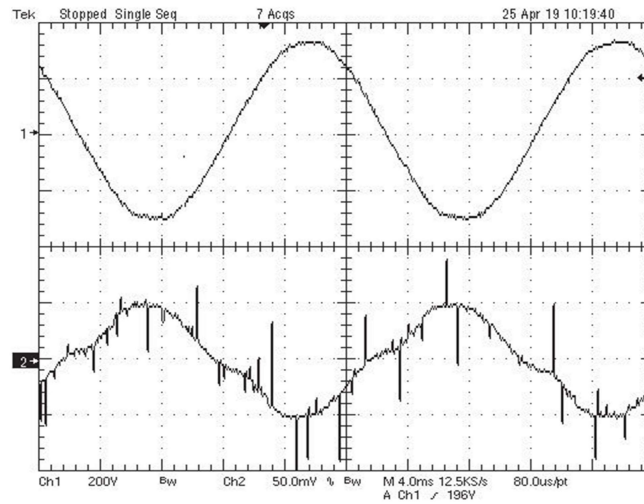


Figure 8. Input line current

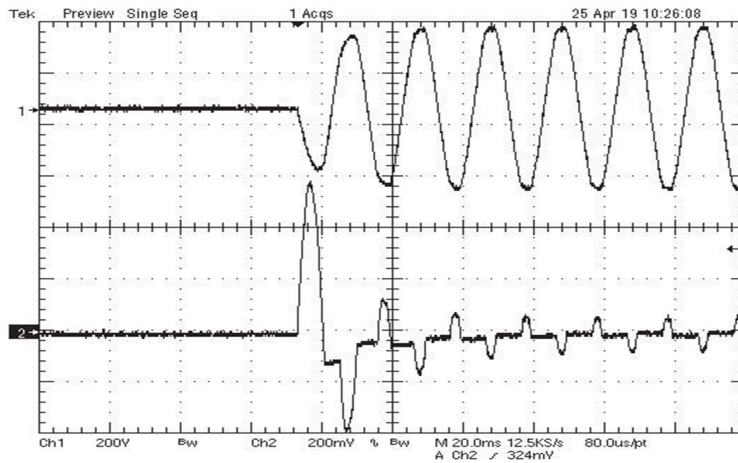


Figure 9. Inrush current

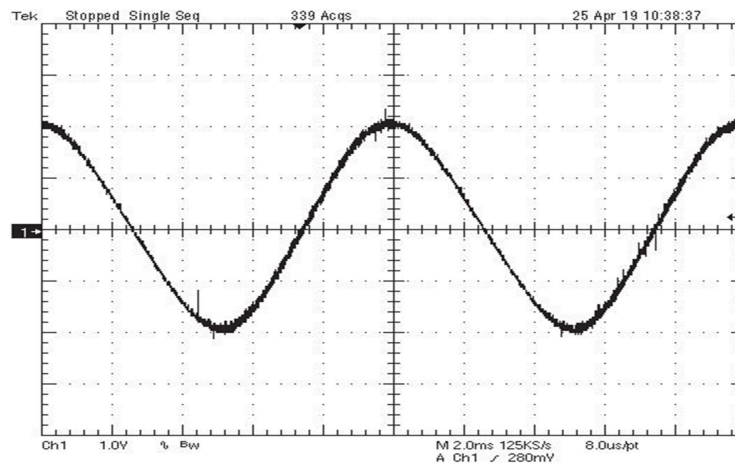


Figure 10. Output ripple

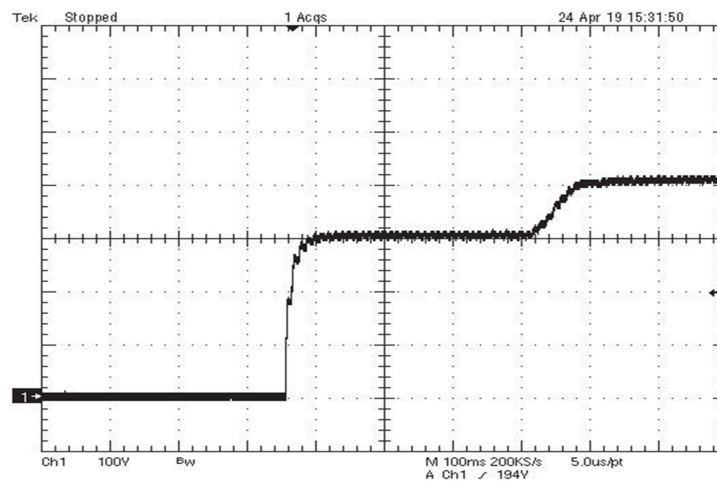


Figure 11. Output voltage start up into full load

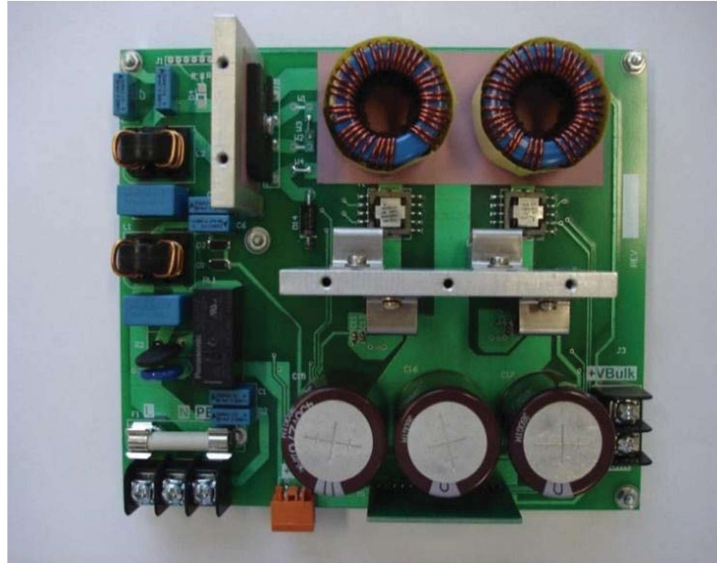


Figure 12. The converter prototype



Figure 13. Experimental setup in the lab

5. Conclusions

In this paper the design and realization of a two phase interleaved PFC converter with GaN FETs and SiC diodes is presented. Calculations and experimental results are presented. The prototype was built and tested. The results verified that the efficiency can go over 98%. Further increase in efficiency is possible by switching to Bridgeless PFC converter topology [6], in order to eliminate the losses of the rectification bridge.

Acknowledgement

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