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# A Novel Interleaved Bridgeless SEPIC Converter With Synchronous Rectifier for Multiple Applications

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**ABSTRACT**

*A new isolated interleaved SEPIC converter feeding synchronous factors rectifier for HVDC and wireless power transmission, and Power factor correction applications are explained and analyzed in this paper. Various converter configurations, such as boost, buck, a combination of buck-boost, cuk, and recently SEPIC, have been used to rectify power factor through the output of bridge rectifier circuit. To enhance the power changeover operation of a proposed system, a modified multilevel inverter is connected through an isolated $(LC)^2$ Synchronous rectifier. This unit can productively improve the SEPIC at wider range output with the ripple-free operation. Further, zero voltage switching (ZVS) is introduced to the synchronous rectifier to reduce the device's operational losses. The mathematical model simplification of the concerned system thus produces the duty cycle with an output feedback control circuit. MATLAB/Simulink is employed for the verification of theoretical analyses and an FPGA controller is used as the experimental setup to validate the simulation setup.*

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**Keywords:** SEPIC, Multilevel Inverter, Isolation Transformer, Rectifier, Resonant Circuit

## 1. Introduction

*An Electrical power distribution system contains numerous Power conversion steps prior reaching to consumer applications. Excellence in Power system operations and applications has become a critical issue, especially when the mode of supply is changed from AC-DC or DC-AC using Converters, as this powerful transformation in electrical buildings leads to electrical Power conversion losses, which in turn increases heat, injecting harmonics, and finally resulting in a decrease in Power factor and efficiency. [1-4]. As a result, Power electronics technology continues to advance, and Power electronics converters are now used in a wide range of commercial and industrial applications. Likewise, the market is more concentrated on this converter and the challenges are progressively increasing [5-6]. The terms of minimal size, lower cost, and superior performance indexes in the converter became more attractive in the market.*

*Classical building blocks of low voltage AC supply to high voltage DC output are accomplished in sequential stages whereby Converters are being employed in the first stage or rectifying the AC source and improving the Power factor[7-9]. In the mid-stage, a DC-to-DC converter is utilized to regulate the rectified DC voltage followed by isolation along with rectification in the final stage. Various Converter configurations, such as boost, buck, a combination of buck-boost, cuk, and recently SEPIC, have been used to rectify Power factor through the output of Bridge rectifier circuits.[10]. By considering the most efficient performance and the wider range of control in Power factor correction, the Buck-Boost and Boost Converter Configurations are paid more attention from the Low to the Higher range of Power and Voltage [10, 11]. Because of the natural boost of voltage performance, the Step-down or buck of voltage over the line voltage of the AC supply is measured up to 400 V [12]. Even though, the poor power factor performance o the buck and boost converter is due to the output voltage being lesser than the nominal value and dead-time effect. The major issue of the SEPIC is low output in voltage harmonics[13,14].Under unbalanced grid conditions, a Bridgeless Power factor correction (PFC) converter is used to compare fuzzy self-tuning (FST), sliding mode control (SMC), and Conventional Proportional–Integral (PI) control methods.*

*The incorporated SEPIC converter is employed to comfort the input current ripple components and work through the incessant or intermittent conduction method. The PWM signals are assured to the Converter with a broader range of frequency to regulate the SEPIC switching devices [15-17]. Further, the altered Diode bridge Five-level inverters are employed to enhance the output and also to reduce the harmonic alteration of the input of the Isolated transformer [18, 19]. The LC resonant circuit has advanced the Output voltage of Isolation, which is associated with the capacity through the Synchronous rectifier. The Synchronous rectifier Converts the AC to DC and regulates the voltage, which is given to the load without disturbing the input [20, 21].*

## 2. Literature Review

*Various approaches Interleaved Bridgeless SEPIC Converter with Synchronous Rectifier for multiple applications. This section describes the Literature survey for tracking the maximum power under different partial loading conditions.*

*Belkamel.H, et.al.[22], have presented, Single-Stage Bidirectional AC–DC Conversion With High-Frequency Isolation Using Interleaved Totem-Pole ZVS Converter Operating in CCM.A new Bidirectional single-stage interleaved Totem-pole Electrolytic capacitors AC–DC converter with high-frequency isolation and a low component count is proposed in this article. The proposed converter performs PFC without the use of a current shaping Control loop, and the Phase-shift angle is the only control variable. Furthermore, due to the small rectified voltage around Zero-crossing, the current spike around the ac main Zero-crossing is avoided in the CCM operation.*

*Wu.Y.E, et.al. [23], have suggested, Three-Winding Coupled Inductor Novel Three-Port Bidirectional DC/DC Converter for Photovoltaic System. This analysis suggested a new Three-port bidirectional converter with a Three-winding coupled inductor and uses it to step up the PV system output to a DC bus or DC load while charging the battery. In order to achieve a High step-up effect, the Converter uses a Three-winding common core coupled inductor and a full-wave doubler circuit on the high-voltage side. Future research directions are determined by analyzing simulated waveforms.*

*Selvi. R.K, et.al.[24], have proposed, speed control of a Switched Reluctance motor using a Particle Swarm Optimization (PSO) tuned Proportional-Integral (PI) controller without a BridgelessLuo converter. Using a Particle Swarm Optimization (PSO) tuned Proportional Integral (PI) controller, This paper proposes a Bridgeless-based Luo converter fed Switched Reluctance Motor drive. The SRM was chosen for the drive because it requires little effort and is simple to develop. Through simulation using Matlab/Simulink design, the proposed Luo converter-based SRM drive framework has been approved.*

*Khan. H.R, et.al.[25], have presented, Brushless DC Ceiling Fan Applications with an Isolated Power Factor Corrected Cuk Converter with Integrated Magnetics. This report outlines a power supply design that includes an AC-DC isolated PFC Cuk converter with integrated magnetics*

*that provides a Single-shunt voltage source inverter for a sensorless BLDC fan motor drive. The Cuk converter uses the Current multiplier method to operate in Continuous Conduction Mode (CCM). The CCM-based current multiplier control loop ensures that the supply current has a near-unity Power factor and low total Harmonic distortion. This system can also be used in conjunction with IT-based controllers to create smart products that can be used for Autonomous control and Power Consumption optimization in the future.*

*Rajan. P, et.al.[26], have suggested, a Three-port Converter with adjustable gain for battery and grid integration in remote location microgrid systems. For the integration of batteries with Single-Phase AC microgrids, this paper proposes a high voltage gain, Bi-directional Buck-Boost port-based hybrid MPC called an energy cushion multiport converter (ECMPC) (SPACMG). A new suggested minimal waste energy management system is used to manage the system for minimal energy waste (MWEMS). An ALTERA field-programmable gate array is used to implement and control the entire system.*

*Sundaramoorthy. S , et.al.[27], have proposed, Average Current Mode Control of Synchronous SEPIC Converters Using Hopfield Neural Networks. Generalized Hopfield Neural Network (GHNN) tuned PI controllers for ACM control of Synchronous Single-Ended Primary Inductance Converters are proposed in this study (SEPIC).The proposed controller's transient and steady-state performance are compared to controllers tuned using the Zeigler Nicholas (ZN) method, Genetic Algorithm (GA), Particle Swarm Optimization (PSO), and Reduced-Order Linear Quadratic Regulator (ROLQR) control scheme for variations in the input voltage, reference voltage, and load using the MATLAB/ Simulink R2015b software tool for variations in the input voltage, reference voltage, and load.*

*Al-Gahtani, et.al. [28], have presented, Under unbalanced and distorted Voltage Supply, Three-phase SEPIC PFC for Three-phase IM drive. Under normal and abnormal supply voltage conditions, this Paper proposes a Three-phase Power factor correction (PFC) for a Three-phase induction motor (IM) drive. This paper introduces a new PFC technique based on the positive sequence components method. The equivalent circuits are mathematically analyzed based on the SEPIC converter's operation modes.*

*S.Sethuraman.S, et.al.[29], have proposed, Synchronous Rectification Modified Topology of a High-Efficiency Bidirectional Type DC-DC Converter.The Non-isolated technique proposes a modified topology for obtaining high efficiency of a bidirectional method of the DC-DC converter. The proposed structure was simulated using MATLAB/Simulink Software, and the results were confirmed using a 12 V/180 V, 200 Watts experimental prototype circuit.*

*Chandan. B, et.al.[30], have suggested An Experiment With A SEPIC Converter Using A BLDC Motor as an example. The open loop experimental examination of a BLDC motor operated by a Single-Ended Primary Inductance Converter (SEPIC) DC-DC converter with no load and on load is demonstrated in this work. Furthermore, it is noted that the inverter's input DC voltage should be constant, which can be accomplished by BLDC motor closed-loop control.*

*Liu. Y, et.al.[31], have presented, ZVS Bridgeless Dual-SEPIC PFC Rectifier with Integrated Inductors, based on Gallium Nitride(GaN).The power factor correction (PFC) of a Gallium Nitride (GaN) based bridgeless dual single-ended primary inductor converter (SEPIC) with an entire input voltage range Zero-Voltage-Switching (ZVS) turn-on for the application of step down AC-DC converters is investigated in this work. The magnetic reluctance modeling for the E-I-E core with the linked inductor, as well as the inductance design for ZVS SEPIC PFC, have been investigated. The converter is more compact thanks to the integrated inductor, which reduces the total Ferrite volume.*

*Singh. B, et.al.[32], have proposed, A Bridgeless Isolated SEPIC Converter is used in a PFC-based EV battery charger. In order to address this problem, this paper presents a bridgeless (BL) Single Ended Primary Inductance Converter (SEPIC) with improved Power quality. As a result, the charger efficiency improves when compared to a traditional BL SEPIC converter. The overall performance of the proposed charger is demonstrated using a variety of operating modes, design equations, simulation-based performance, and experimental validation in both steady state and over a wide range of AC mains voltage fluctuations.*

## 3. Schematic Operation of Proposed System

*A Single-phase AC/DC converter isolated battery charger circuit is shown in Figure 1. The detailed explanation and different modes of operation of the proposed configuration are as follows.*

### 3.1. Circuit Explanation

*As highlighted in Figure 1, the single-phase AC/DC converter has an isolated battery charger circuit. The structure consists of input of AC source connected to interleaved SEPIC converter output which is connected to five-level multilevel inverter structures along with an isolated synchronous rectifier. The power factor interleaved SEPIC is carried two number of power semiconductor switches $S_1$ & $S_2$, inductors $L_1$ & $L_2$, capacitors, & and four diodes &. The SEPIC output DC voltage is collected across the capacitor $C_d$ and it has performed the input of Five-Level, multilevel inverter circuits. At this moment, the voltage is alienated into Positive and Negative by employing the Capacitors $C_{d1}$ and $C_{d2}$. Further, MLI consists of the auxiliary unit of four diodes $D_{a1}$- $D_{a2}$ with auxiliary switch Sa and H bridge circuit of four switches $H_1$- $H_4$.The output is connected to the Synchronous Rectifier through an isolation transformer. The Synchronous Rectifier has combined with four switches R1-R4 and it is connected to the load or battery along with the filter circuit of InductorLp and Capacitor Cp. Therefore, the objective of each unit is to accomplish the SuperiorPower factor in input and converted DC by interleaved SEPIC, to lessen the component harmonic and also to convert the AC waveform from DC by ML1, to isolate and guard against the short circuit with no load condition by isolating the transformer and resonant circuit, in order to reduce the delay by Zero Voltage Switching of the Synchronous rectifier.*

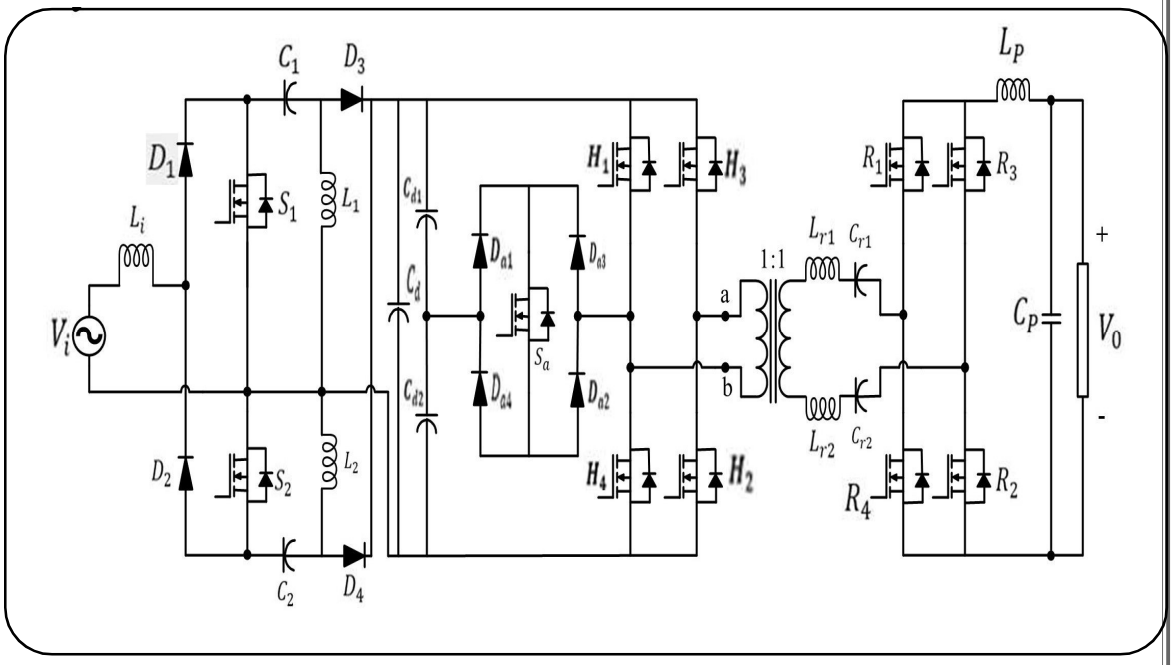



**Figure 1. Proposed Interleaved SEPIC Converter**

### 3.2. Operating Modes

*In order to reduce the mathematical analysis procedure, the above-displayed structure of AC/DC conversion from source to load or endpoint is drawn as a simplified circuit. The voltage output of each unit is an input of a subsequent unit, and it is stated to promote the imperturbable overview. In addition, the output Filter Circuit Lp & Cp is ignored, in which the isolation transformer input to output transformation is consistent because of its 1:1 ratio or ultimate. The incorporated SEPIC converter consumes the two operating modes, firstly, in the Positive half cycle, and secondly, in the Negative half cycle. And during the Positive Half-cycle period, the Switch $S_1$ is closed, and $S_2$ is turned off and vice versa.*

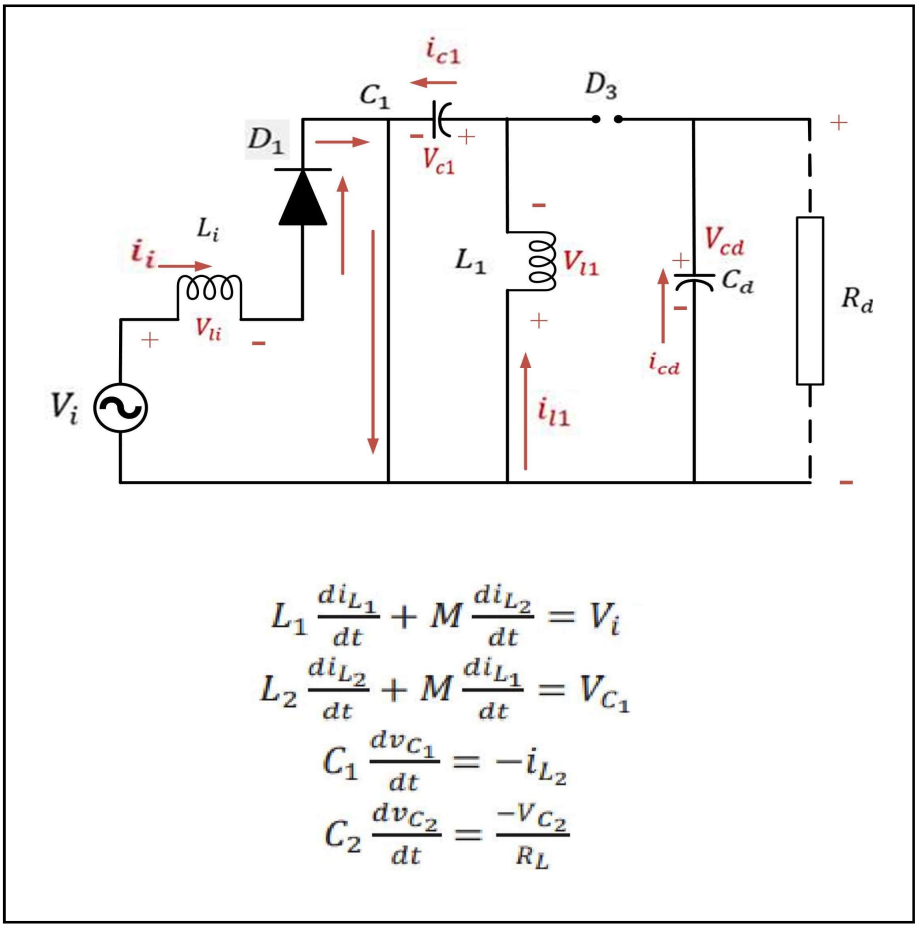



**Figure 2. SEPIC converter operation in mode 1**

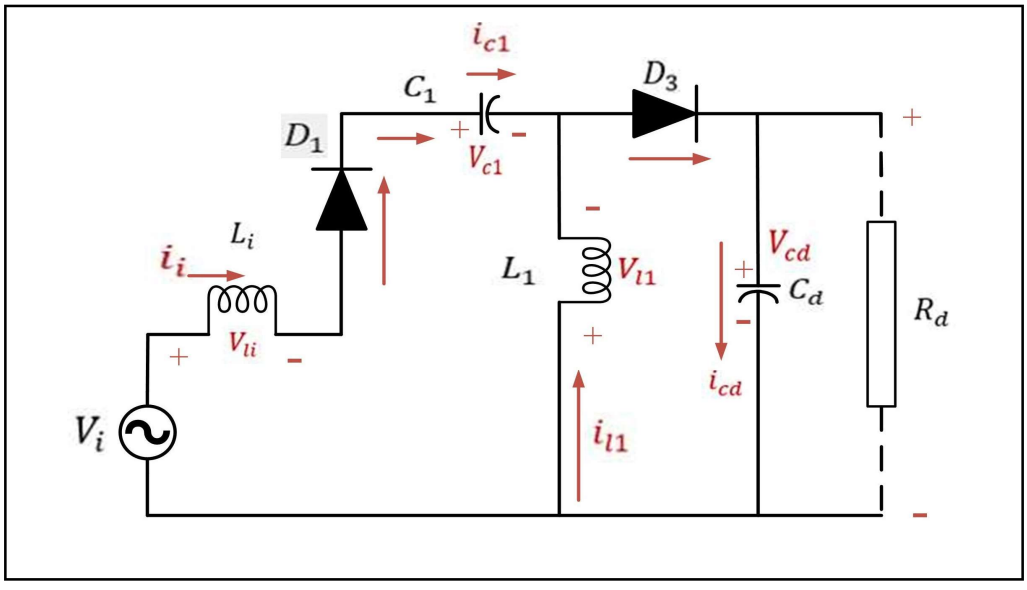



**Figure 3. SEPIC converter operation in mode 2**

$$L_1 \frac{di_{L_1}}{dt} + M \frac{di_{L_2}}{dt} = V_i - V_{C_1} - V_{C_2}$$

$$L_2 \frac{di_{L_2}}{dt} + M \frac{di_{L_1}}{dt} = -V_{C_2}$$

$$C_1 \frac{dv_{C_1}}{dt} = i_{L_1}$$

$$C_2 \frac{dv_{C_2}}{dt} = i_{L_1} + i_{L_2} - \frac{V_{C_2}}{R_L}$$

*The positive cycle of supply $V_i$, the current through the Inductor $L_i$, diode $D_1$, switch $S_1$ is turned on, Inductor $L_1$, Capacitor $C_1$, diode $D_3$, and Capacitor $C_d$.TheInductor current il1 and the Capacitor current $i_{c1}$ are increased linearly from Zero in the Reverse direction whereas the capacitor $C_d$ voltage polarity is given in Figures 2 & 3. The voltage across $C_d$ is divided equally by $C_{d1}$ and $C_{d2}$ and the capacitors have performed the Source of the Five-level inverter.*

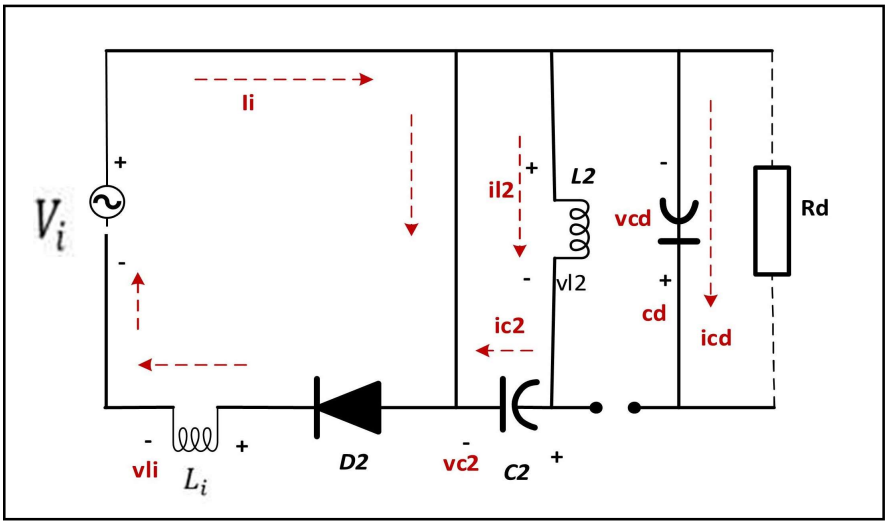



**Figure 4. SEPIC converter operation in mode 3**

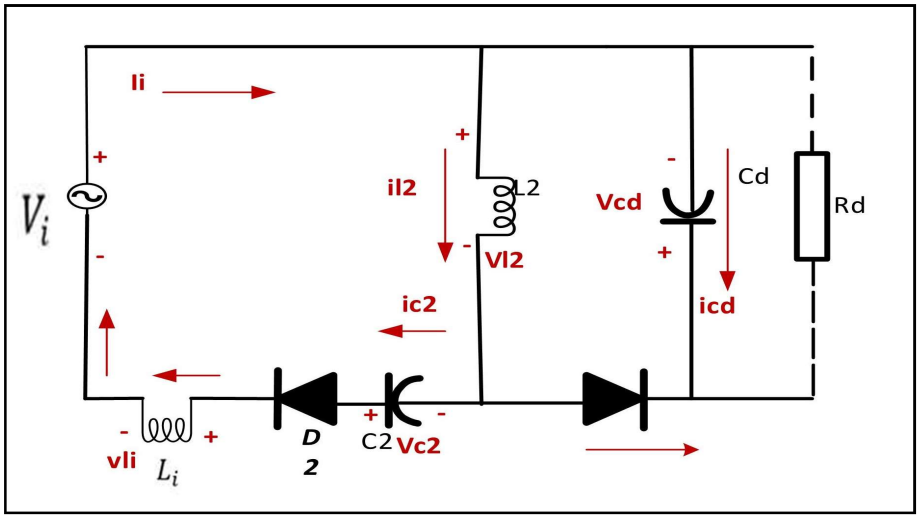
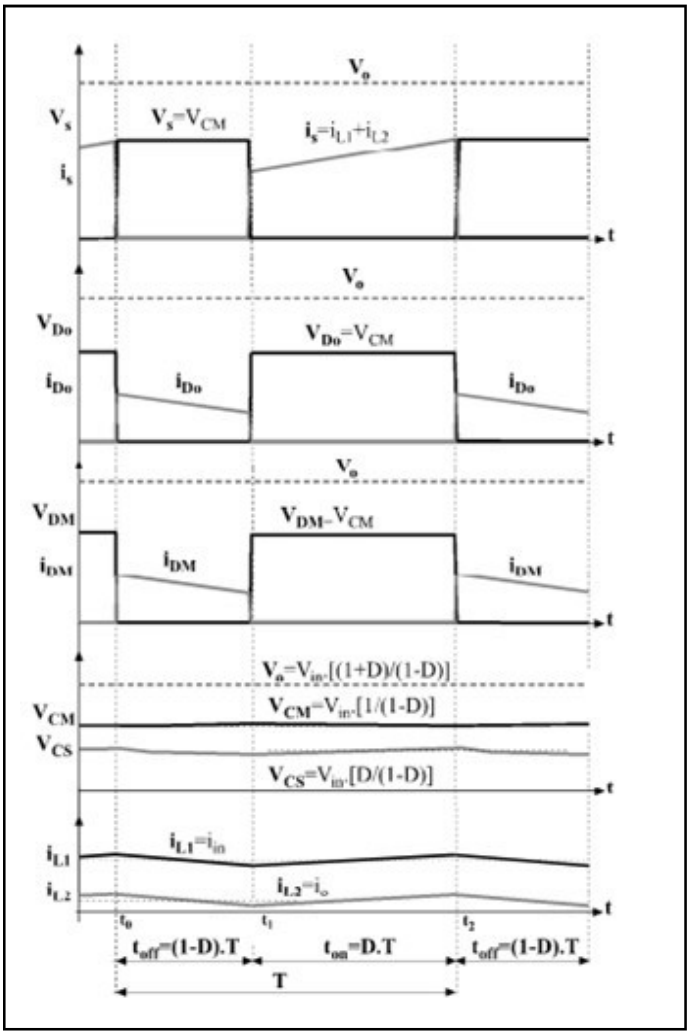



**Figure 5. SEPIC converter operation in mode 4**

*In this mode, the source $V_i$ is a Negative half cycle and the switch $S_2$ is turned on, the diodes $D_2$ and $D_4$ are forward bias, in which the current through the $L_2$ inductor is $i_{l2,}$ and the $C_2$ capacitor $i_{c2}$ is raised into a Positive direction linearly. The input inductor Li current is augmented incomparable to the voltage and the source diagonally to the capacitor $C_d$ which residues identical to the preceding model. Therefore, the voltage split through the capacitors $C_{d1}$ and $C_{d2}$ is known as unchanged polarity, and the direction of current in interleaved SEPIC is shown in Figures 4 & 5.*

**SEPIC converter main Theoritical waveform**

*The SEPIC converter main theoretical waveform is given. Supply voltage and current, capacitor voltage and current, inductor voltage and current is generate the waveforms in sepic converter*




**Main theoretical waveforms**

**Converter Designing Equations**

***Duty cycle calculation:*** *The duty cycle of the sepic converters and the parasitic elements in the circuit determine how much the voltage is stepped up or down by the sepic converters. An ideal sepic converter's output is given by,*

$$V_0 = \frac{D * V_i}{1 - D} \qquad (1)$$

*However, parasitic losses, such as the diode drop VD, are not taken into account. This completes the equation*

*However, parasitic losses, such as the diode drop VD, are not taken into account. This completes the equation.*

$$V_0 + V_D = \frac{D * V_i}{1 - D} \quad (2)$$

*This becomes,*

$$V_0 + V_D = \frac{D * V_i}{1 - D} \quad (3)$$

*When the input voltage is at its lowest, the maximum duty cycle occurs. The duty cycle maximum is*

$$D = \frac{V_0 + V_D}{V_0 + V_i + V_D} \quad (4)$$

***Inductor Selection**: Allow the peak-to-peak ripple current to be approximately 40% of the maximum input current at the minimum input voltage when determining the inductance. The ripple current flowing through inductors of equal value L1 and L2 is given by,*

$$\Delta I_L = I_i X 40\% = I_0 x \frac{V_0 x 40\%}{V_{i\min}} \quad (5)$$

*The inductor value is calculated by*

$$L_1 = L_2 = L = \frac{V_{i\min}}{\Delta I_L x f_{sw}} x D_{\max} \quad (6)$$

where *D* max is the duty cycle at the minimum *V* in and *fsw* is the switching frequency. To ensure that the inductor does not saturate, the peak current in the inductor is given by

$$I_{L1peak} = I_o x \frac{V_o + V_D}{V_{i\min}} x(1 + \frac{40\%}{2}) \quad (7)$$

$$I_{L1peak} = I_o x \frac{V_o + V_D}{V_{i\min}} x(1 + \frac{40\%}{2}) \quad (8)$$

Due to mutual inductance, if L1 and L2 are wound on the same core, the value of inductance in the equation above is replaced by 2L. The value of the inductor is calculated as follows:

$$L_1' = L_2' = \frac{L}{2} = \frac{V_{i\min}}{2x\Delta I_L x f_{sw}} x D_{\max} \quad (9)$$

**Power MOSFET Selection**: The minimum threshold voltage Vth(min), on resistance RDS(ON), gate-drain charge QGD, and maximum drain to source voltage, VDS, are the parameters that govern MOSFET selection (max). Based on the gate drive voltage, logic level or sublogic-level threshold MOSFETs should be used. Vin + Vout is the maximum switch voltage. The peak switch current is calculated as follows:

$$I_{Q1peak} = I_{L1peak} + I_{L2peak} \quad (10)$$

*The RMS current through the switch is given by*

$$I_{Q1rms} = I_0 \sqrt{\frac{(V_0 + V_{i\min} + V_0)x(V_o + V_D)}{V_{i\min}^2}} \quad (11)$$

$$P_{Q1} = I_{Q1rms}^2 x R_{DSON} x D_{\max} + (V_{i\min} + V_0) x I_{Q1peak} x \frac{Q_{DO} x f_{sw}}{I_G} \quad (12)$$

*Conduction loss (as shown in the first term of the above equation) and switching loss (as shown in the second term) are included in PQ1, the total power dissipation for MOSFETs. The gate drive current is IG. The RDS(ON) value, which is typically found on the MOSFET data sheet, should be chosen at the maximum operating junction temperature. Ascertain that the total conduction and switching losses do not exceed the package ratings or the total thermal budget.*

***Input Capacitor Selection**: At the input of the SEPIC, there is an inductor. As a result, the current waveform at the input is continuous and triangular. The inductor ensures that ripple currents in the input capacitor are kept to a minimum. The RMS current in the input capacitor can be calculated as follows:*

$$I_{cinrms} \frac{\Delta I_L}{\sqrt{12}} \quad (13)$$

*The RMS current should be handled by the input capacitor. Although the input capacitor is not critical in a SEPIC application, a good quality capacitor with a value of 10 F or higher would prevent impedance interactions with the input supply.*

***Output Capacitor Selection**: The inductor charges when the power switch Q1 is turned on, and the output current is supplied by the output capacitor. The output capacitor's RMS current is*

$$I_{corms} = I_0 \sqrt{\frac{V_0 + V_D}{V_{i\min}}} \quad (14)$$

*The output ripple is directly controlled by the output capacitor's ESR, ESL, and bulk capacitance. Assume that the ESR is responsible for half of the ripple and that the capacitance is responsible for the other half.*

$$ESR \le \frac{V_{ripple} x 0.5}{I_{L1peak} + I_{L2peak}} \quad (15)$$

$$C_0 = \frac{I_0 x D}{V_{ripple} x 0.5 x fsw} \quad (16)$$

*Tantalum, polymer electrolytic, and polymer tantalum capacitors, as well as multi-layer ceramic capacitors, are recommended for surface mount applications.*

***Output Diode Selection**: The output diode must handle the peak current and reverse voltage. In a SEPIC, the diode peak current equals the switch peak current. At its lowest point, the reverse Q1(peak) voltage.*

$$V_{RD1} = V_{i\max} + V_{o\max} \quad (17)$$

*The output current multiplied by the forward voltage drop of the diode equals the diode's power dissipation. In order to reduce efficiency loss, Schottky diodes are recommended.*

***SEPIC Coupling Capacitor Selection**: The RMS current, which is given by, determines which SEPIC capacitor, Cs, should be used.*

$$I_{corms} = I_0\sqrt{\frac{V_0 + V_D}{V_{i\min}}} \qquad (18)$$

*In relation to the output power, the SEPIC capacitor must be rated for a large RMS current. The SEPIC capacitor's voltage rating must be higher than the maximum (23) input voltage. On Cs, the peak-to-peak ripple voltage.*

$$\Delta V_{cs} = \frac{I_o x D_{\max}}{C_s x f_{sw}} \qquad (19)$$

### 3.3 Five level Inverter

*The five-level multilevel inverter is shown in Figure 1. Consists of an auxiliary and H-bridge circuit. The ChargedCapacitor voltages of $C_{d1}$ and $C_{d2}$ act as a source of MLI. The five-level output waveform across the isolation transformer primary side is generated, and the level of voltages are $+V_{d1}$; + ($V_{d1}$ + $V_{d2}$); 0; - $V_{d2}$,-($V_{d1}$ + $V_{d2}$). In a positive cycle the output, the first level current direction is $C_{d1}$, $H_3$, isolation transformer A to B, and the auxiliary circuit $D_{a3}$; $S_a$ and$D_{a4}$ as shown in Figure 1. Meanwhile, the second level in the positive cycle is achieved by $C_{d2}$; $C_{d1}$; $H_3$, in which the isolation transformer A to B and $H_4$ is shown in Figure 6.*

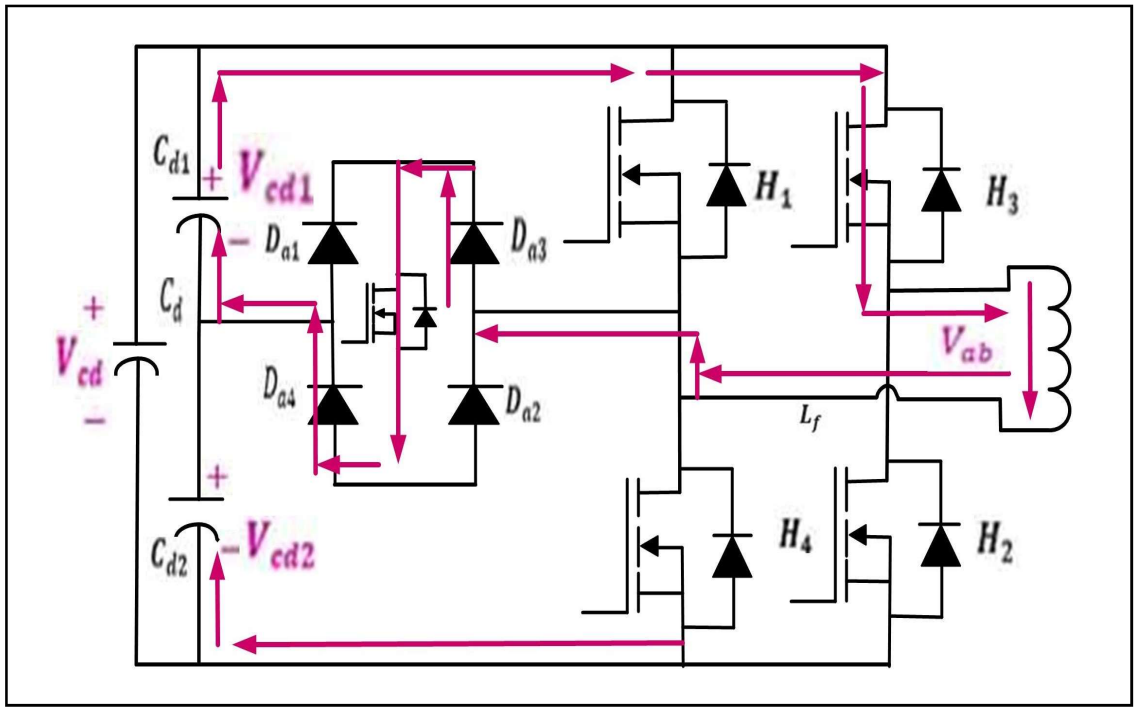



**Figure 6. Switching mode operation of the Five-level inverter**

Similarly, the Negative half cycle of the two levels is achieved by $C_{d2}$;$D_{a1}$; $S_a$;$D_{a2}$ isolation transformer B to A, and $H_2$ for the first level, and the second level current direction is $C_{d2}$;$C_{d1}$; $H_1$ and the Isolation Transformer B to A and $H_2$ as shown in Figures 6-9 respectively. The Zero Voltage across ato b is obtained by keeping switches are kept in a turned-off condition.

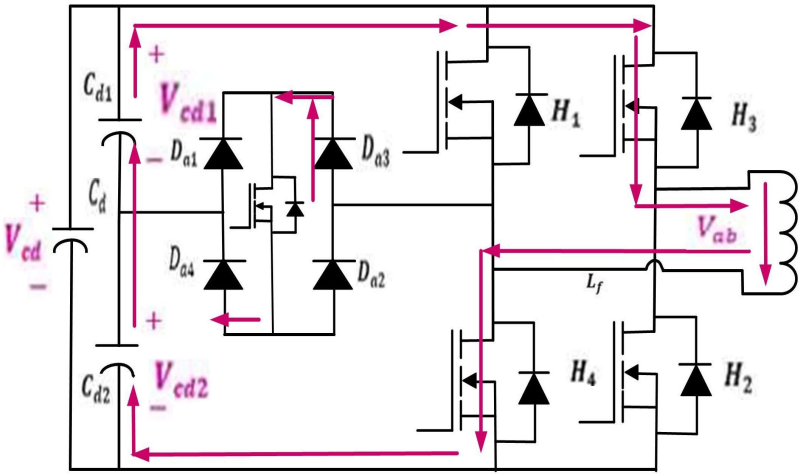



**Figure 7. Switching mode Five-level inverter**

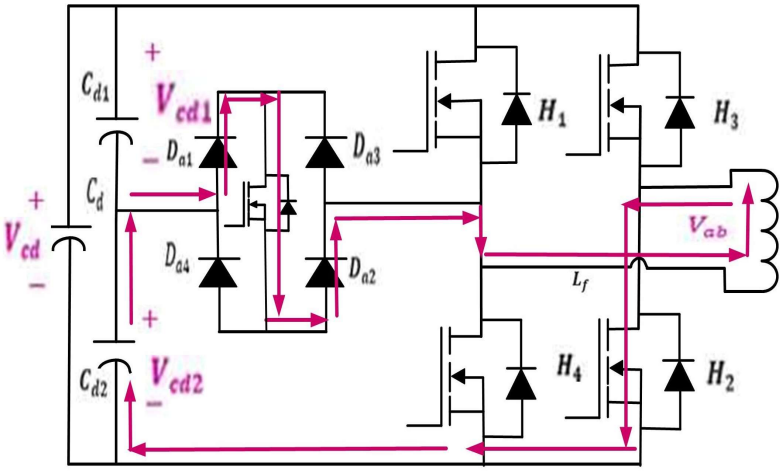



**Figure 8. Switching mode Five-level inverter**

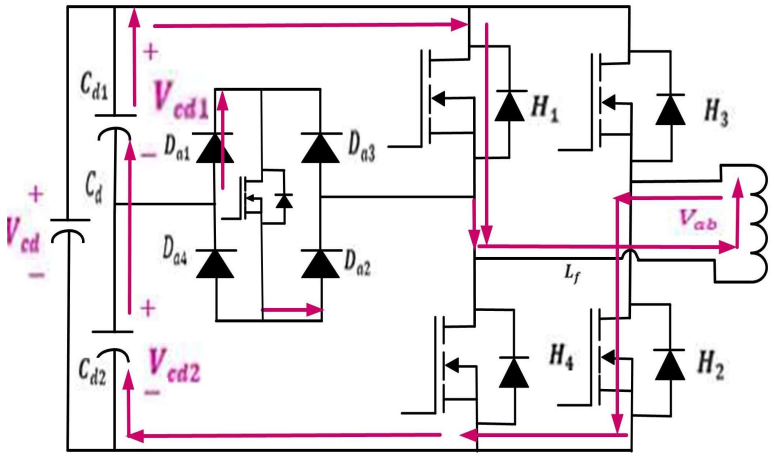



**Figure 9. Switching mode of theFive-level inverter**

### 3.4. Synchronous Rectifier

*The two switching pairs and the synchronous H-bridge rectifier circuit are produced to switch on and off by regulating the devices as presented in Figures 10 & 11. Even though the voltage through the resonant tank output is zero, the rectifier voltage output is also zero. It means that the Current over the Rectifier devices (MOSFET) from the trench to a source of R1- R4 is zero.*

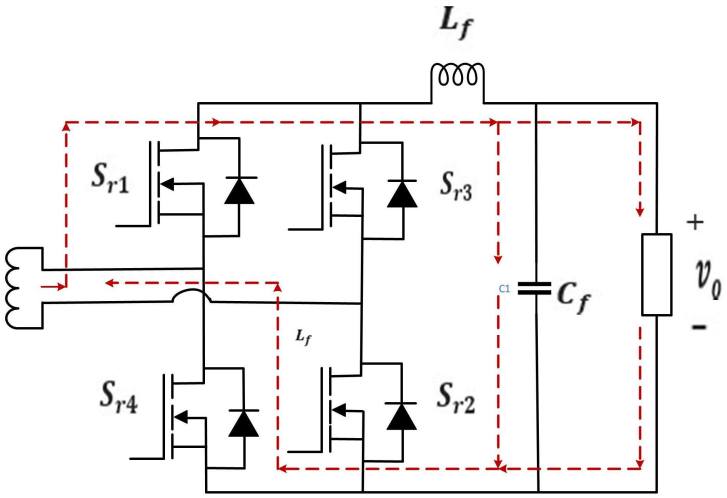



**Figure 10. Synchronous H-bridgeless rectifier**

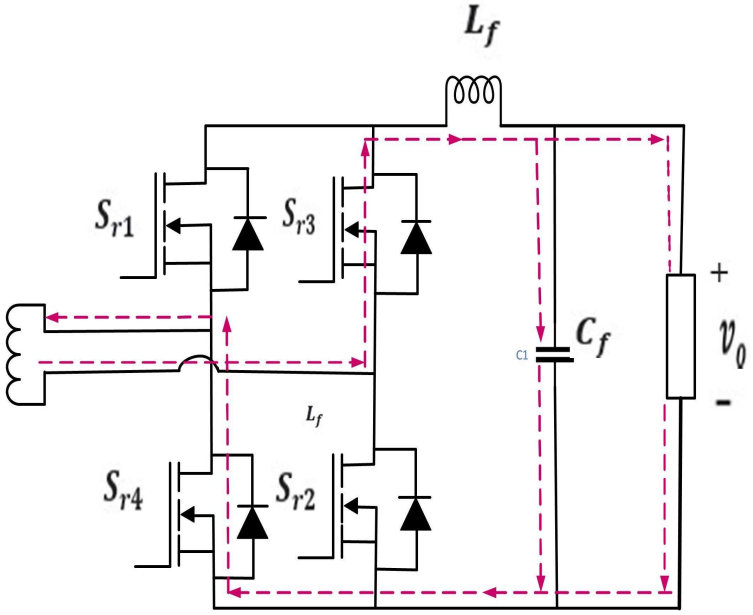



**Figure 11. Synchronous H-bridgeless rectifier**

*The proposed converter structure is different from the Conventional converter*

***SEPIC converter:*** *AC supply is used in the SEPIC converter. one Capacitor connected in parallel and inductor connected in series of the switch. capacitor connected to the series of the inductor and inductor parallel to the switch-1.Resister RL is connected parallel to the C2.*

***Conventional converter:*** *DC supply is used in the Conventional converter. Two capacitors are*

*connected to the ground. S1 and S4 connected in Series and S2 and S3 connected in Series then two set of switches connected in parallel.*

### 3.5. Isolated Secondary side LC

*The isolated transformer is employed to segregate the MLI and rectifier circuits. The supreme Isolation transformer is designated in this recommended structure and the reverberating tank circuit is associated with the transformer's secondary side. The Resonant circuit generates current lags and secondary side transformer voltage, while the key qualities of the resonant circuit include brand for Switching on the MOSFET of Synchronous rectifier at zero voltage switching (ZVS), which decreases switching losses and EMI conflicts.*

### Applications of Interleaved SEPIC converter

SEPIC converters are used in many applications they are, Including Battery-operated equipment *and hand-held devices. NiMH chargers. LED lighting applications. DC power supplies with a wide range of input voltages.*

## 4. Steady-state Modelling of Proposed System

*In this unit, steady-state mathematical modeling is recommended to regulate the passive component assessment and also to advance the performance. Throughout the Positive cycle, $S_1$ is turned on and the diode $D_3$ is not conducted.*

$$\left.\begin{aligned} L_i \frac{di_i}{dt} &= v_i \\ L_1 \frac{di_{l1}}{dt} &= -v_{c1} \\ C_1 \frac{dv_{c1}}{dt} &= i_{l1} \\ C_d \frac{dv_{cd}}{dt} &= \frac{v_{cd}}{R_d} \end{aligned}\right\} t_1 T_s \tag{1}$$

*During the Positive cycle $S_1$ is opened and the Diode- l is forward biased.*

$$\left.\begin{aligned} L_i \frac{di_i}{dt} &= v_i - v_{c1} + L_1 \frac{di_{l1}}{dt} \\ L_1 \frac{di_{l1}}{dt} &= v_{cd} \\ C_1 \frac{dv_{c1}}{dt} &= i_i \\ C_d \frac{dv_{cd}}{dt} &= i_i + i_{l1} - \frac{v_{cd}}{R_d} \end{aligned}\right\} t_2 T_s \tag{2}$$

*During the positive cycle $S_2$ is turned on and the diode $D_4$ is not conducted.*

$$\left.\begin{aligned} -L_i \frac{di_i}{dt} &= v_i \\ L_2 \frac{di_{l2}}{dt} &= v_{c2} \\ C_d \frac{dv_{cd}}{dt} &= \frac{v_{cd}}{R_d} \\ C_2 \frac{dv_{c2}}{dt} &= i_{l2} \end{aligned}\right\} t_3 T_s \tag{3}$$

*During the positive cycle $S_2$ is opened and the diode $D_4$ is forward biased.*

$$\left.\begin{aligned} L_i \frac{di_i}{dt} &= v_i - L_2 \frac{di_{l2}}{dt} - v_{cd} \\ L_2 \frac{di_{l2}}{dt} &= v_{c2} \\ C_2 \frac{dv_{c2}}{dt} &= i_i \\ C_d \frac{dv_{cd}}{dt} &= i_i + i_{c2} - \frac{v_{cd}}{R_d} \end{aligned}\right\} t_4 T_s \qquad (4)$$

*The five-level inverter output voltage*

$$\begin{aligned} &V_{ab} = (-H_k) * k * 0.5 C_d \frac{dv_{cd}}{dt} \; if \\ &S_a = on \;\&\; H_k = -1, for\; k > 2 \end{aligned} \qquad (5)$$

*The transformer ideal and the leakage inductance were assumed as negligible. The secondary side resonant tanks upper and lower are*

$$z_{s1} = z_{s2} = j\left(\omega L_{rx} - \frac{1}{\omega C_{rx}}\right) \; x = 1 \; or \; 2 \qquad (6)$$

$$Zs = Zs1 + Zs2 \qquad (7)$$

$$\omega = \frac{1}{\sqrt{\omega L_{rx} C_{rx}}} \qquad (8)$$

$$f = \frac{1}{2\pi\sqrt{L_{rx} C_{rx}}} \qquad (9)$$

*The resonant current frequency*

*The synchronous rectification voltage equation from resonant tank is*

$$V_r = 2 i_r Z_s + V_o \qquad (10)$$

## 4. Results and Discussion

*To prove the mathematical development of AC-DC Power Converter performance, the Simulation and Hardware setup were analyzed with the same parameters and the specifications are listed below.*

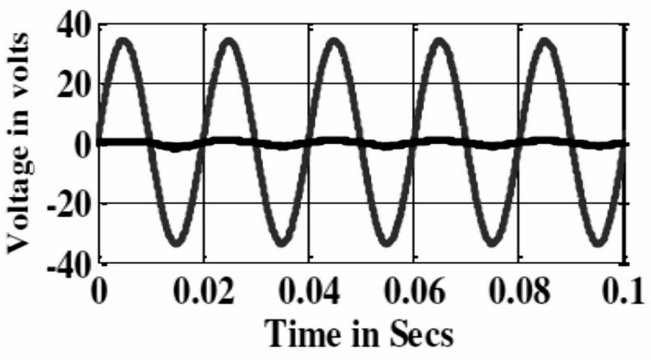



**Figure 12. Input voltage and current**

*The survey of voltage and time is shown in Figure 12. Sinusoidal wave is created in positive and negative side.*

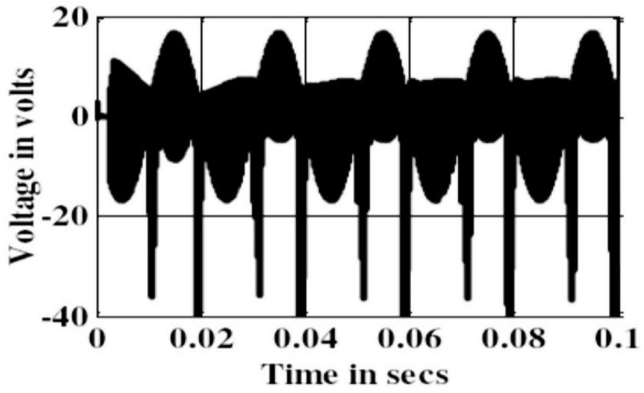



**Figure 13.Voltage across source inductor**

*The survey of voltage across source inductor and time is shown in figure-13. Some Power is stored in the Inductor, voltage across source inductor value is measured*

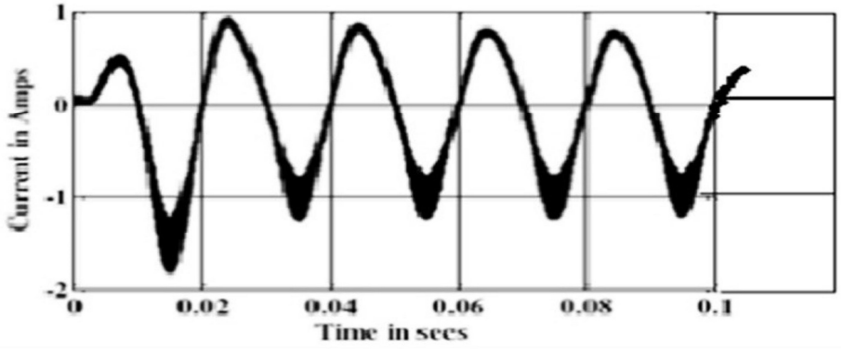



**Figure 14. The survey of source inductor Current -Time is shown in figure14**

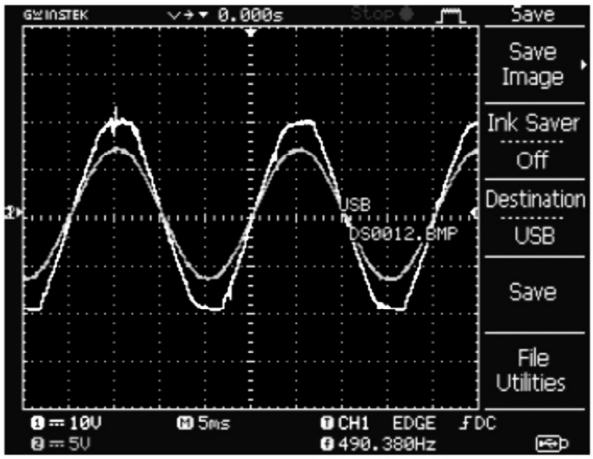



**Figure 15. Experimental source voltage and current**

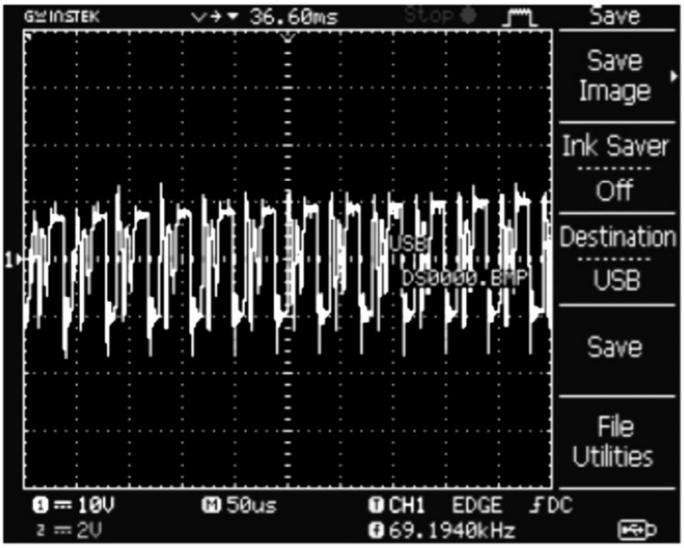



**Figure 16. Experimental source Inductor Voltage**

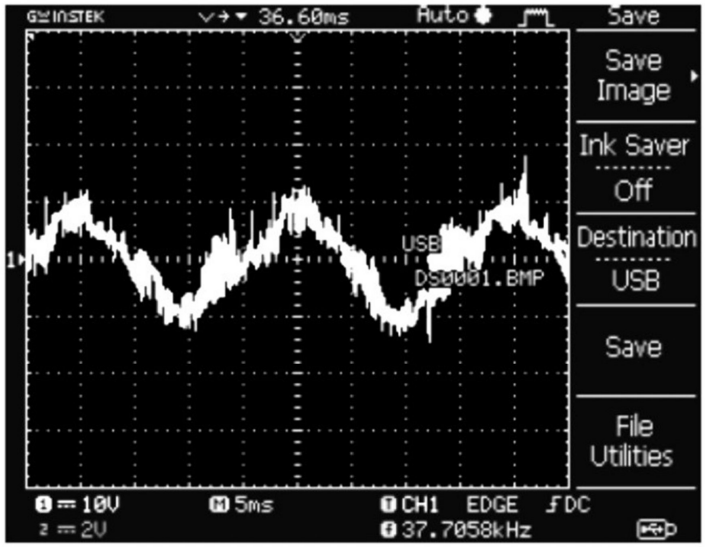



**Figure 17. Experimental source Inductor current**

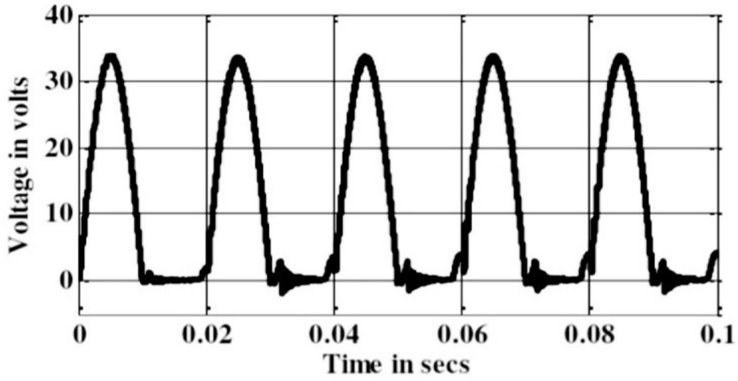



**Figure 18. Simulated capacitor $C_1$ voltage**

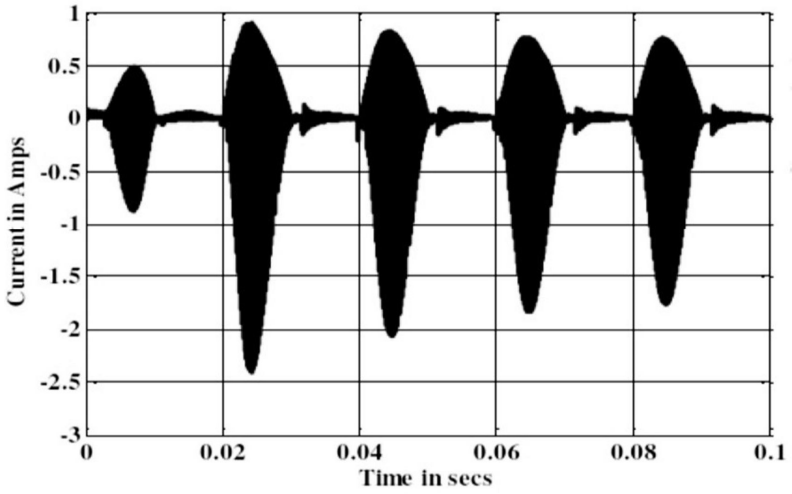



**Figure 19. Simulated capacitor C1current**

| Components | Ratings |
|---|---|
| Source Voltage | 12V,50Hz |
| Source Current | 1 A |
| Inductors | 1 mH/5A |
| Capacitors | 4.7 F/63V |
| Capacitor(in SEPIC output) | 2000 F/50V |
| Isolation transformer | 1:0.5 |
| Output load (PMDC drive) | 12V,1500rpm,1.5A |
| Switching frequency | 25kHz |
| Output power | 18W |
| Switching devices(all) | IRF250 |
| Diodes(all) | FR207 |

**Table 1. Simulation and Experimental Setup Parameters**

*In the above-mentioned Converter system, the input voltage is 24V, 50Hz AC supply, and the Output voltage is converted to 12.08V across the PMDC motor as a load, as shown in Figures 12-51. Figures 12-17. Demonstrates the Interleaved SEPIC converter source sides the source inductor voltage and current waveforms. The input supply Power factor is 0.999 and it is purely sinusoidal.*

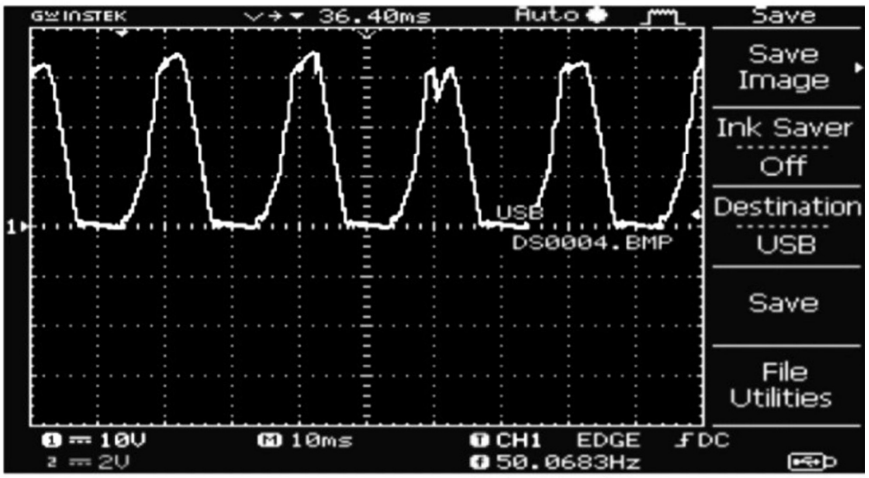



**Figure 20. Experimental capacitor $C_1$ voltage**

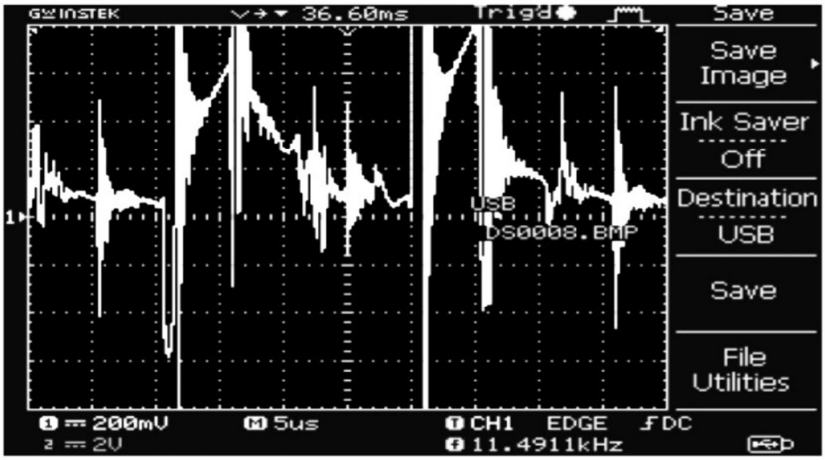



**Figure 21. Experimental capacitor $C_1$ current**

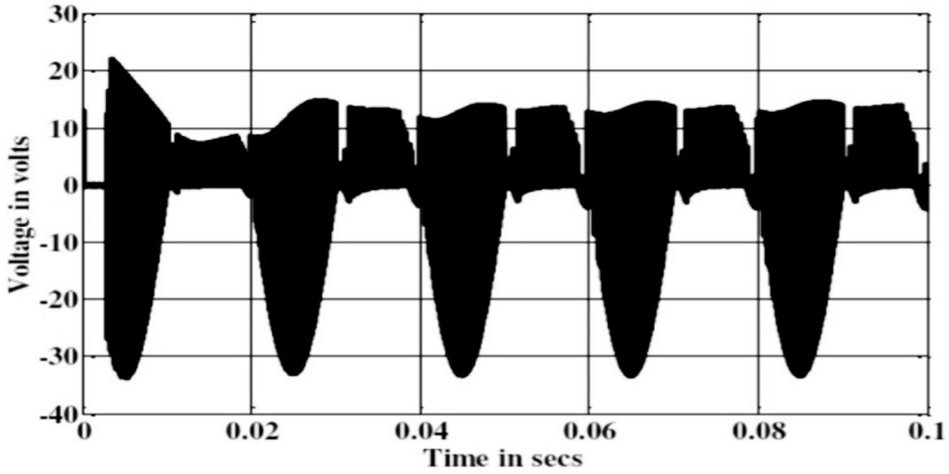



**Figure 22. Simulated inductor $L_1$ voltage**

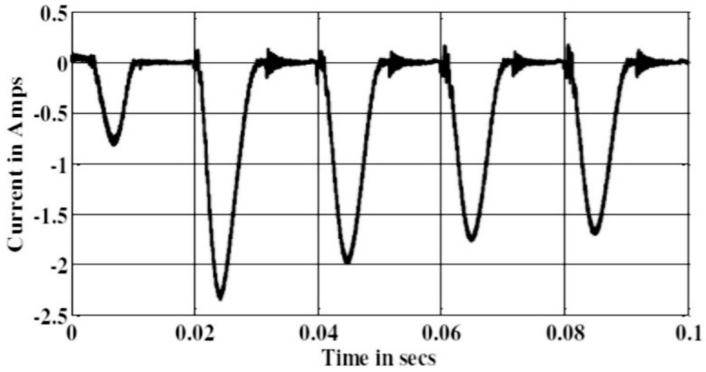



**Figure 23. Simulated inductor $L_1$ current**

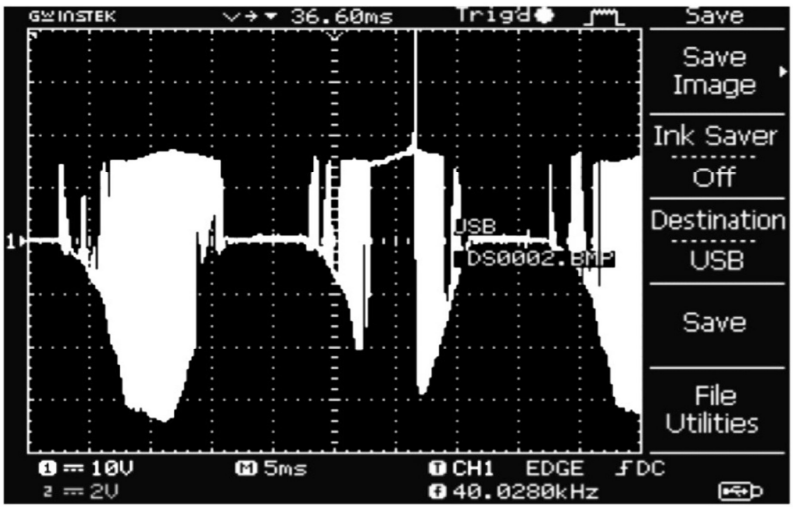



**Figure 24. Experimental inductor $L_1$ voltage**

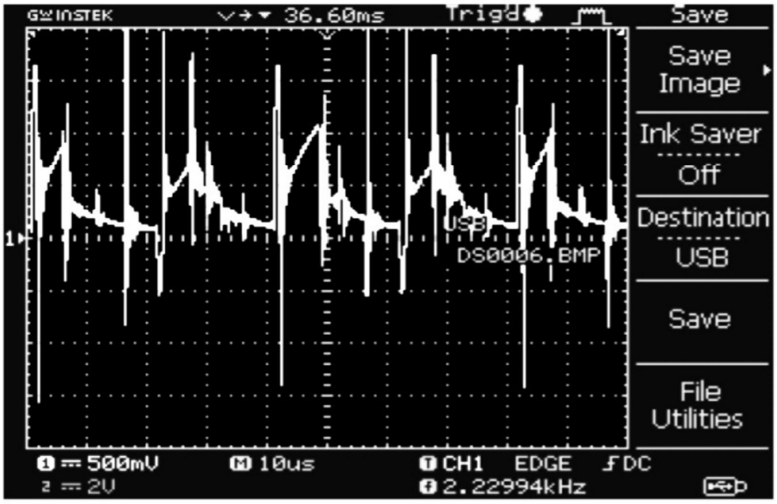



**Figure 25. Experimental inductor $L_1$ current**

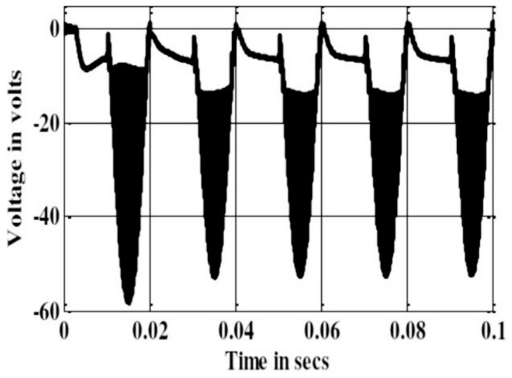



**Figure 26. Simulated capacitor $C_2$ voltage**

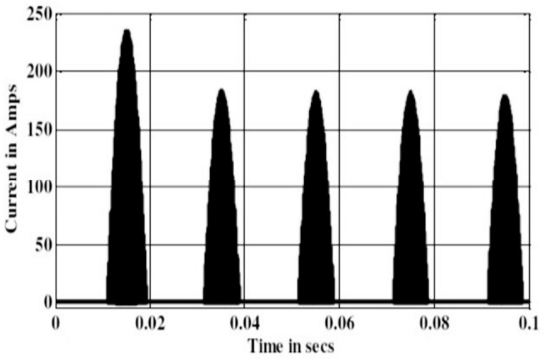



**Figure 27. Simulated capacitor $C_2$ current**

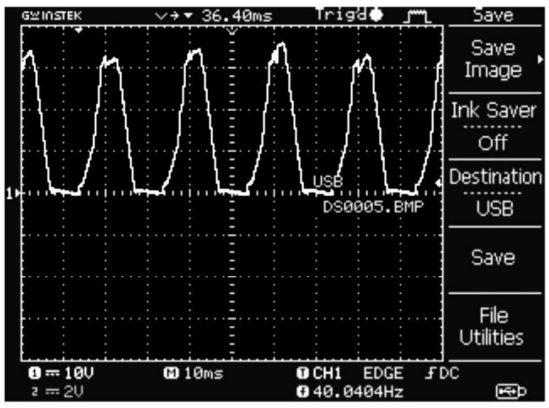



**Figure 28. Experimental capacitor $C_2$ voltage**

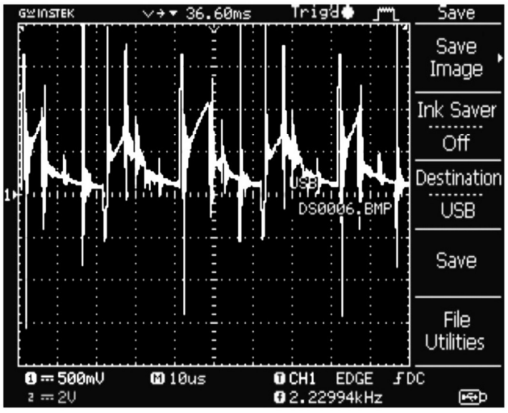



**Figure 29. Experimental capacitor $C_2$ current**

*The waveforms contained the spikes in the measurement at the Source in Inductor output. Figures Inverter Highlight the capacitor C1 charges the voltage and the current waveform. The Capacitor C1 waveform is available at a positive cycle only. Figures 22-25 explain the negative cycle waveform of inductor L1 charges and discharging cycle in simulation and experimental.*

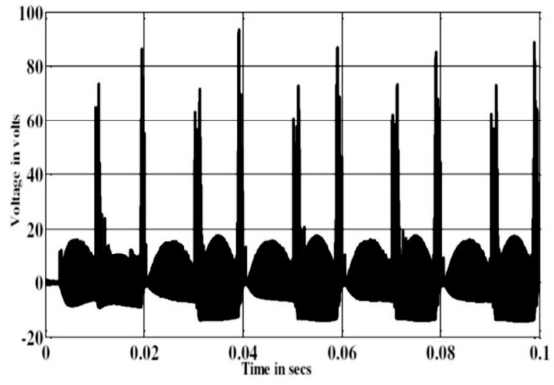



**Figure 30. Simulated inductor L2 voltage**

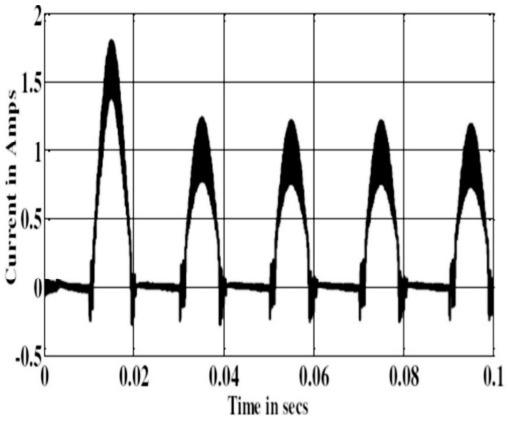



**Figure 31. Simulated inductor L2 current**

*Due to the Inductive effect, the spikes and nonlinearity charges and discharging are potential cycles. The explanation of simulated and experimental results of Figures 18-21, during the positive cycle of source and the Figures 22-33 are interleaved SEPIC $L_2$& $C_2$ waveforms charges*

*operation during the negative cycle.*

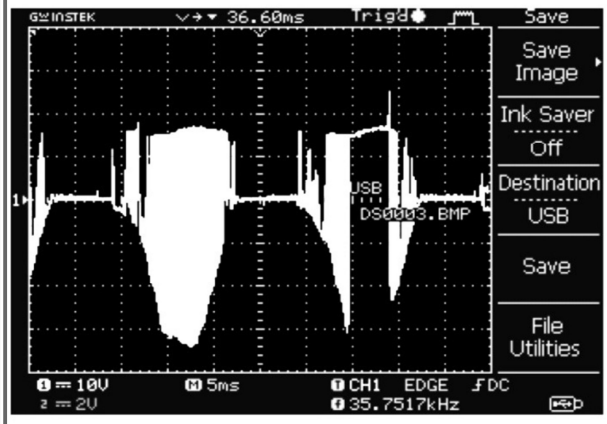



**Figure 32. Experimental inductor $L_2$ voltage**

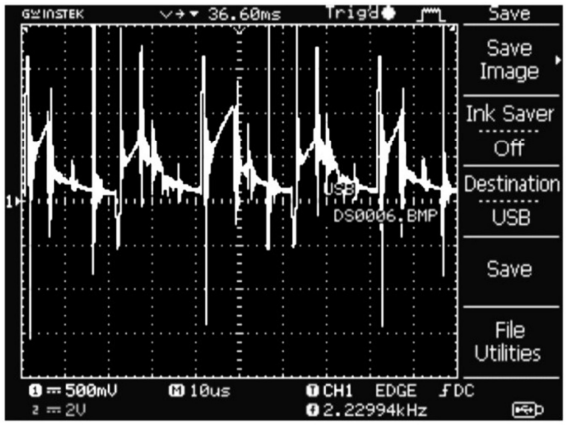



**Figure 33. Experimental inductor $L_2$ current**

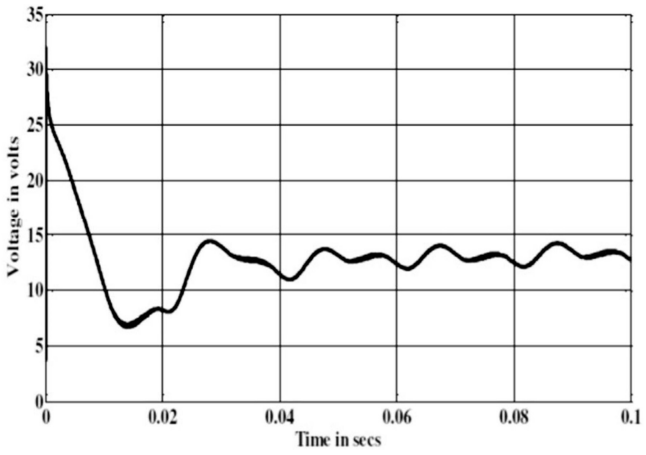



**Figure 34. Simulated capacitor Cd voltage**

The survey of capacitor voltage and time is shown in figure. Voltage is starts from (0to 32) Suddenly voltage is decreased (0.01,7).Some fluctuation is occurs in voltage final value is (0.1,13).

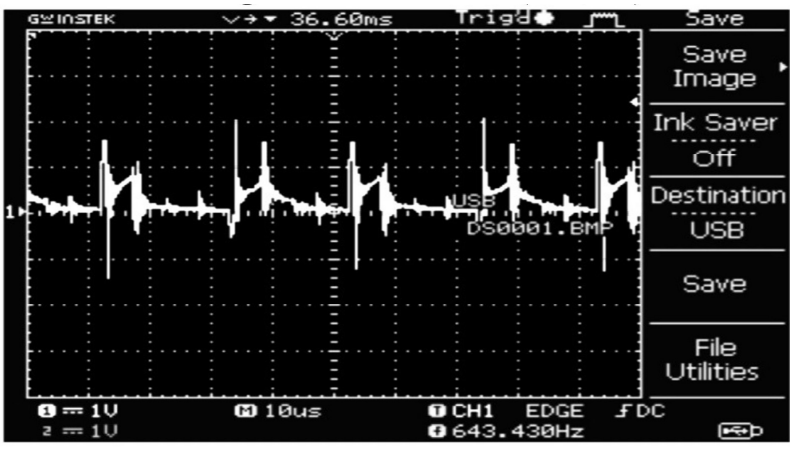



**Figure 35. Experimental capacitor Cd current**

*The survey of Voltage and Time is shown in figure. Positive and Negative side five level voltage is measured. positive side voltage level is 20 and negative side voltage level is -20.*

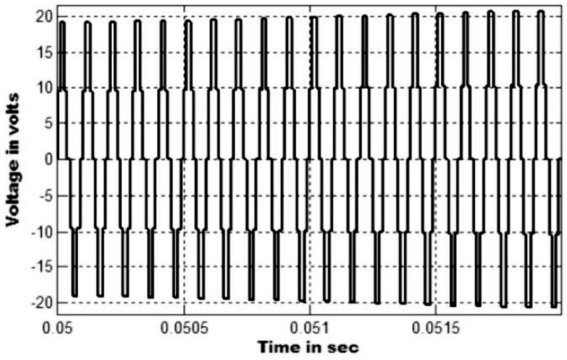



**Figure 36. Simulated FiveLevel inverter output voltage**

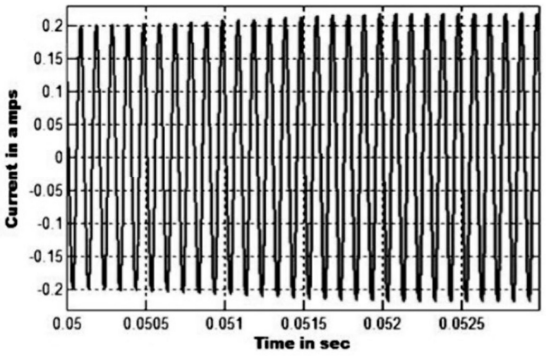



**Figure 37. Simulated Five Level Inverter Output Current**

*The survey of Five-Level Inverter Current and Time is shown in figure. Positive and Negative side is measured. Positive side current level is 0.2 and Negative side current level is -0.2. time level after 0.0515 small changes is occur in current value positive is above 0.2 and negative is above -0.2.*

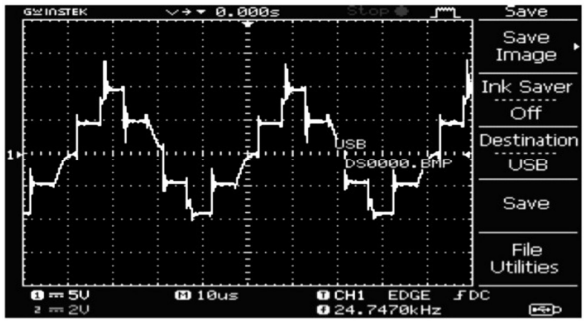



**Figure 38. Experimental five level inverter output voltage**

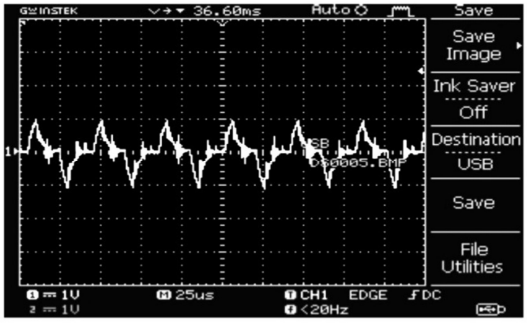



**Figure 39. Experimental Five Level inverter output current**

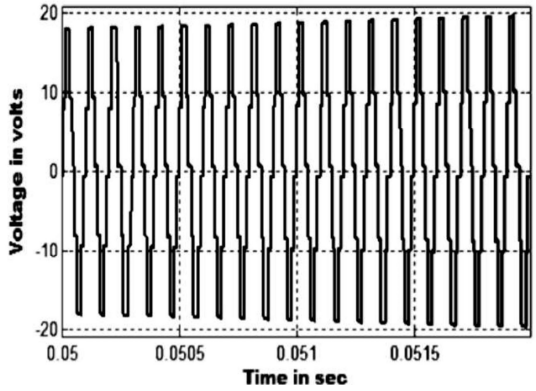



**Figure 40. Simulated isolation transformer output voltage**

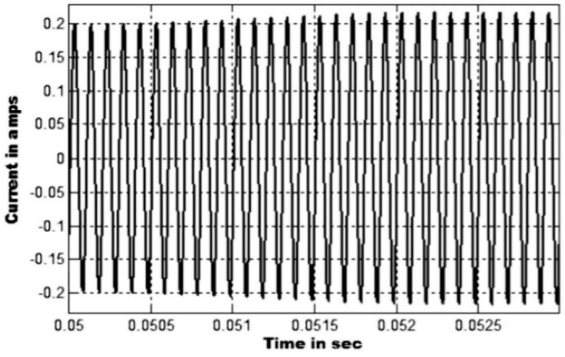



**Figure 41. Simulated Isolation Transformer Output Current**

*Figure 34 provides the simulated SEPIC converter output (VCD) voltage waveform and the output voltage is 13V. Figure 35 explains the 0.42 A current output of interleaved SEPIC converter. At the same time, the experimental output v voltage is 14V across the capacitor Cd and the*


**Figure 42. Experimental isolation transformer output voltage**


**Figure 43. Experimental isolation transformer output current**

*interleaved SEPIC converter's output current is 0.36A.*

*The Primary voltage of the Isolation transformer and the output voltage of five-level inverter is 9V, 0.65 A, and 9.3V, 0.58 A are obtained by hardware as shown in Figures. 36-39. The five-level inverter output voltages are comprised of the distortions and it is followed in the secondary also which is displayed in Figures 40-43.*

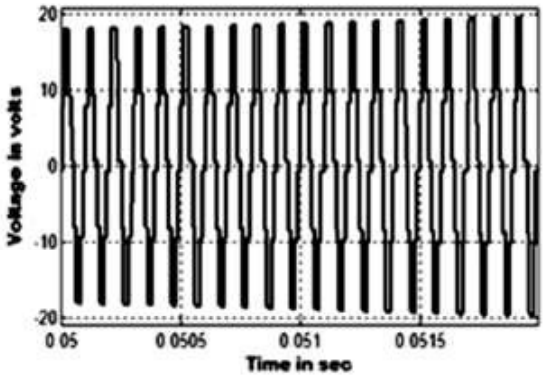



**Figure 44. Simulated LC resonant output voltage**

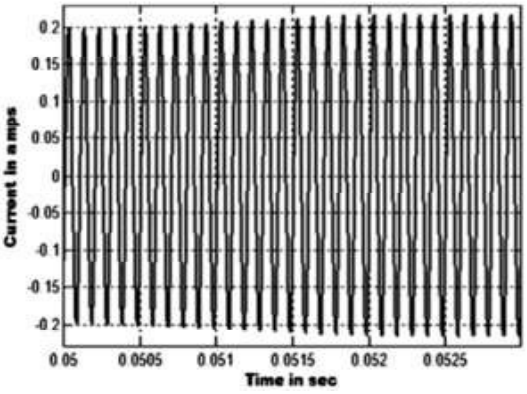



**Figure 45. Simulated LC resonant output current**

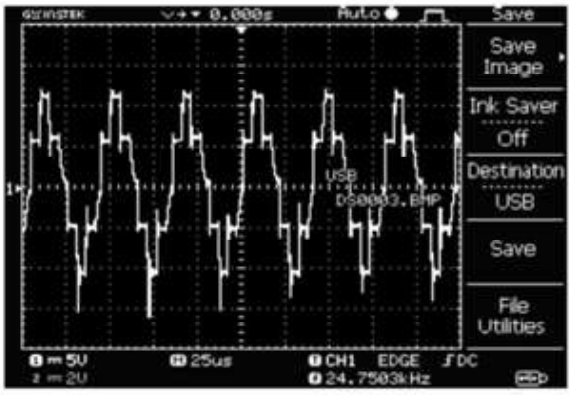



**Figure 46. Experimental LC ResonantOutput Voltage**

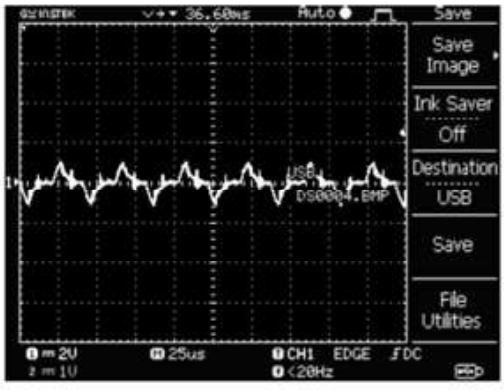



**Figure 47. Experimental LC Resonant output current**

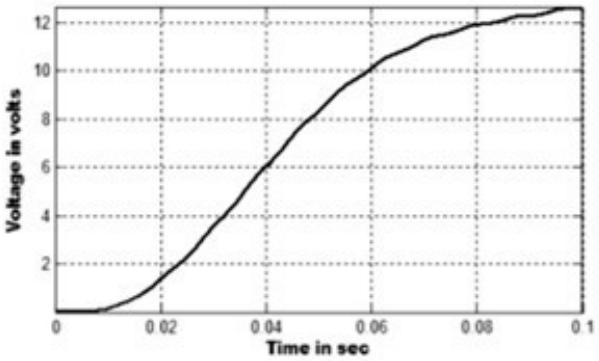



**Figure 48. Simulated load output voltage**

*The survey of load output voltage and time is shown in figure. Voltage is increasedand Time is also gradually increased*

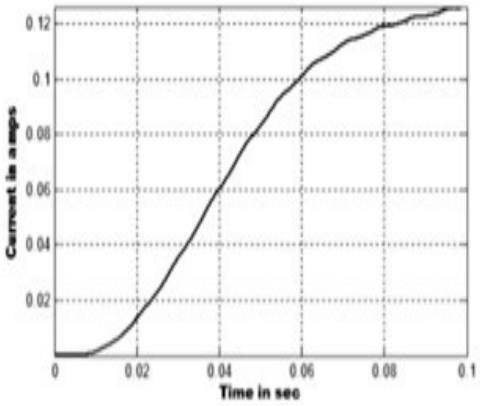



**Figure 49. Simulated load output current**

*The Isolation Transformer voltage waveform is not changed in the shape and it is reduced to 1:1 or ideal as shown in Figures 40 & 42. The LC resonant circuit is constantly operating under the Resonant Frequency which cuts out the spikes output from the Isolation Transformer. These actions of the LC component have significantly improved the overall performance and Efficiency as shown in Figures 44-47.*

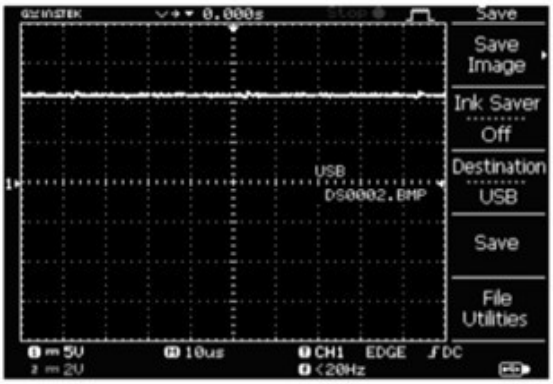



**Figure 50. Experimental Load Output voltage**

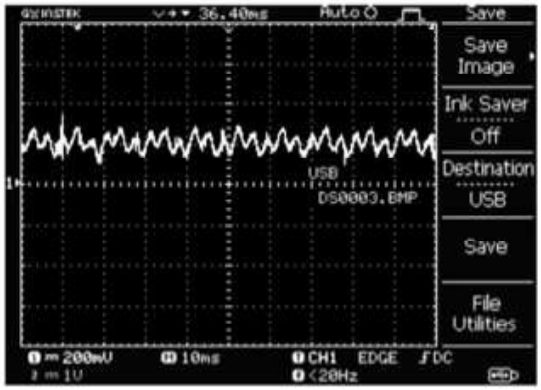



**Figure 51. Experimental Load Output Current**

**Figure 52. Experimental Set-up**

*Two MOSFETs, three inductors, three diodes, and three capacitors make up the main circuit. The L3 inductor is a toroidal type inductor. Two switches operate in 180-degree phase shifts in alternate cycles. C1 and C2 also Operate in a cycle that alternates. This alternate cycle will be combined by the output diode.*


**Figure 53. Gate signal for switch S1**

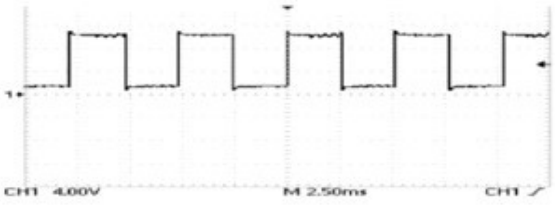



**Figure 54. Gate signal for switch S2**

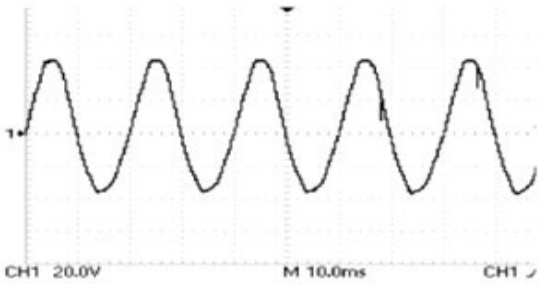



**Figure 55. Prototype input Voltage obtained in DSO**

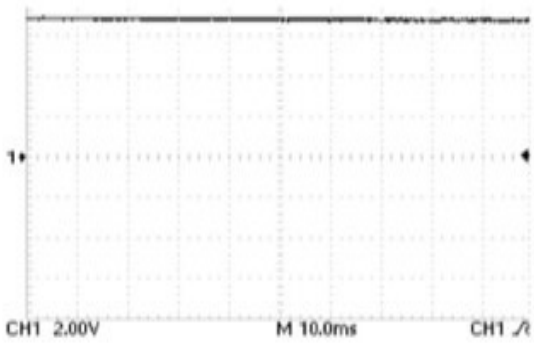



**Figure 56. Prototype output Voltage obtained in DSO**

*Figure 53 and Figure 54. shows the gate pulse for switches in Hardware circuit. Figure 55. and Figure 56.shows the input and output voltage obtained using DSO from hardware circuit*

*The conversion of AC to DC proves the poor performances and the efficiency of the conventional rectifier circuits due to frequent switching and conduction losses in the circuit. The synchronous rectifier reduced the Power losses in a device by operating at Zero vo Voltage or Current switching methods as shown in Figures 44-51.*

*Similarly, Figures 49 & 51 show that the Output Current is 0.35A and 0.33A in simulation and experimental respectively. The SynchronousRectifies the Switches Turned On and Off at Zero voltage when the isolation secondary side voltage is zero. It is extensively reduced to the device losses and switching losses. The output voltage or PMDC motor voltage when the current of simulation and experimental setup results are shown in Figures.48 & 50 respectively.*

*The output voltage is obtained as 12.8V for simulation and 11.5V for experimentally. Figure 52 shows that the prototype experimental setup is designed as in table 1 parameters. The comparison of gain of different dc-dc converters with the proposed interleaved SEPIC converter is given in table 2. It is known that the value of gain varies with the value of the duty cycle. The maximum gain is attained if the gain value is maximum. But the highest value of gain increases the switching stress and power loss. The below table represents the gain value of converters for the duty cycle of 0.9.*

| **Converter type** | **Gain value** |
|---|---|
| Boost converter | 1.5 |
| CUK converter | 2 |
| BL Boost converter | 4 |
| SEPIC converter | 4 |
| Bridgeless CUK converter | 6 |
| Interleaved bridgeless SEPIC converter | 12 |

Table 2. Gain comparison

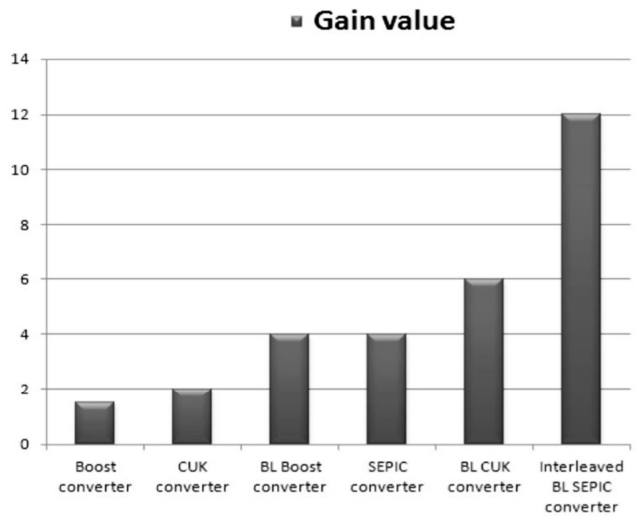



**Figure 57. Gain Comparison**

## 5 . Conclusion

*Finally, this current research pretends the performance of an AC-DC Power Converter configuration by an Isolated Synchronous Rectifier of the comprehensive structure. In which, the mathematical modeling has been corroborated by the experimental setup. A Bridgeless Interleaved SEPIC converter is smeared to astound the drawbacks of conventional bridge topologies. The simulated and experimental results have established the alterations of the MLI were reduced to 6% of THD. As a final point, the hardware outcomes are the witness and the power factor is 0.999, and its approximate unity.*

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