Look Ahead Clock gating using an Auto gated Flip flop for Low Power Application

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ABSTRACT: *We propose new technique for clock gating. Clock gating is helpful for reducing power consumed in digital systems. There are three technique used, viz., (i) Synthesis Based method (ii) Data driver Method, and (iii) Auto gated flip flop (AGFF). The Auto gated Flip flop can be distributed in the clock distribution network. Clock distribution uses current other than voltage by giving global clock. With auto gated flip flop, it is used for power sowing. Clock gating can be tested in current mode pulsed flip flop which enable* urrent-Mode Pulsed Flip-Flop with Enable *(CMPFFE) using 48nm CMOS technology. In the Look Ahead Clock Gating (LACG) computers, the clock signals at one cycle ahead of time. The Flip flop depends on the present cycle in LACG. This model can be characterized by power saved in FF. This technique is based on a data to clock togging. Majority of the FF fall in positive Region. Experimentation shows that the industry-scale data displays 22.5% reduction of clock power.*

Keywords: Look-Ahead Clock Gating (LACG), Auto-Gated FFs (AGFF), Current-Mode Pulsed Flip-Flop with Enable (CMPFFE).

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1. Introduction

All portable Electronic devices require long battery life. Power consumption is the major problem in electronic products. Low power design is responsible to tolerate the power consumption clock signals which are responsible for 30% to 60% of the total dynamic (switching) power consumption. There are many techniques used to reduce dynamic power. Clock gating is one of the predominate techniques to reduce power. When a Logic unit is clocked, its upcoming sequential elements receive the clock signal whether clock signal is needed or not. By means of clock gating Logic gates, Logic system architecture is employed at all stages where we know that the above method is synthesis based.

Synthesis based clock gating is used in EDA tools. The abducing clock pulses can be measured by data to clock toggling Ratio. The clock enacting signals are derived by Logic synthesis. It is shown in data toggle in very Low rate compared to the gated clocks. The clock load thus consumes more power.

In order to address data driven clock gating, the clock signal driving a FF is gated when there is no change in the clock cycle. The relation between data driver-based and synthesis-based clock gating method shown in the Arithmetic circuits. The data driver gating is explained in Fig. 1. The disabled clock can be find in the next cycle using a FF by Xoring the output with present input; then the output will display in next cycle. The output of XOR gate is OR Ed together for joint gating. Data driven gating is suffered by a short time- window. Clock gating is explained in the Fig 2 and the design methodology is very difficult in data driven method. In order to maximize the power saving, flip flop is grouped together. The main applications are unknown and the redundant clock pulses may increase in specific application. The IP providers who are delivering RIT code need to broadcast the gating circuitry as per customer. It requires marinating different version of the same IP.

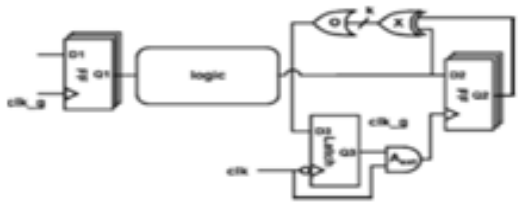

Figure 1. Circuit implementation of data – driven clock gating

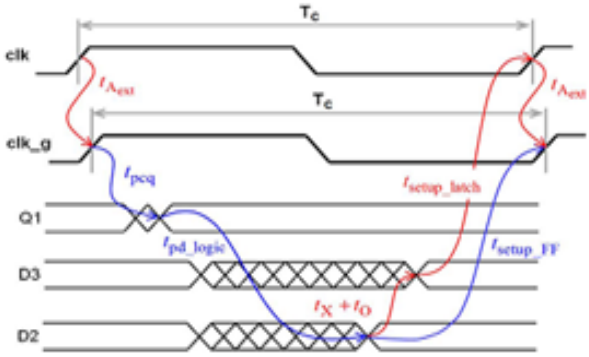

Figure 2. Sequencing of gating logic in data driven clock gating

In this paper, we propose Look Ahead Clock Gating (LACG). It shows clock enabling signal at each flip flop. It depends on present cycle data same as data driven gating AGFF and the data driven enable full clock signal. Data Driven requires optimization of FF. The simplified gating implementation is Auto gated Flip flop.

The Rest of the paper discussed about the optimization and implementation LACG section develops power saving models.

2. Overview of Autogated Flip Flop

The basic circuit diagram of Autogated flip flop is shown in the figure 3. The flip flop master latches are transparent in falling edge of the clock. The output must be stable. When master latch is opaque, then EXOR gate shows batch change in state.

Power reduction was proposed for register based small circuits. The counters are the input for each Flip flop. There are two major draw backs, (i) shows are gated but half of the clock load are not gated; and (ii) Timing constraints are imposed on those flip flop on critical path this avoids gating.

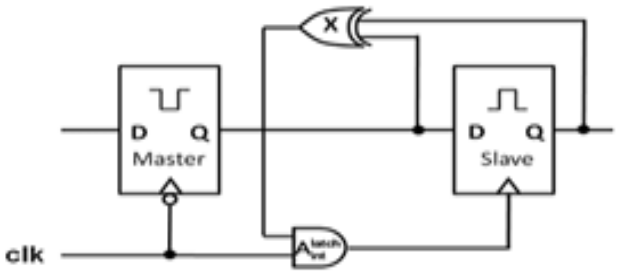

Figure 3. A gated flip-flop

LACG uses AGFF for three goals. In order to stop the clock pulses in master Latch, and making the clock pulse applicable for general design and avoiding timing constraints LACG is based on XOR output. The XOR output is valid only during a narrow window [$-t_{setup}$, t_{ccq}] where t is setup and t_{ccq} are FF's are setup time. If t_{ccq} delay the XOR output and turns to zero, XOR and OR gate are helpful in clock switching.

Figure 4 represents how LACC operators assume FF^{11} as target and FF^{1} as source. The target depends on $K \geq 1$of source FF's. The source FFs can be found by a transversal of the Logic paths for D^{11}. It performs RTL or NOT-list description.

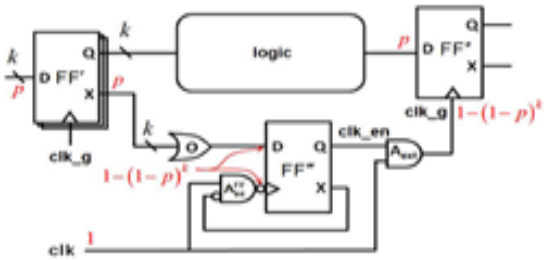

Figure 4. LACG of general logic

Generate the enable signal obtained from t and its validity is t +1. The clock edge falling ad t +0.5 then D^{111} (t+0.5) = $\sum_{x}(o^{11})x(t)$ since FF^{111} is opposite to clock. The signal Q^{111} is stable when the time period is [t + 0.5, t +1]. By using FF for gating, the consumption of power will be its own. In figure 4 identity that FF^{111} is clocked oppositely. Here internal XOR gate will be connected between D^{111} and Q ^{111}. LACG has a full clock cycle in order to evaluate clock. For implementation, require clock enabling signal. LACGs are derived from the figure 5.

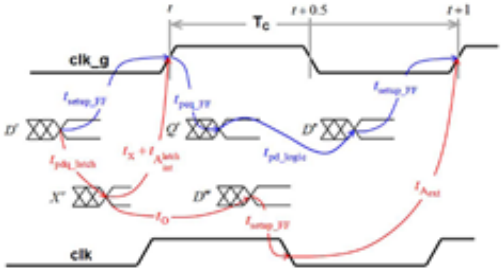

Figure 5. Timing sequence of LACG clock gating

$$t_{pdq}\ latch + t_{Aint}\ Latch + tx \leq t\ setup\ FF \qquad (1)$$

Where t_{pdq}, t_x and t_A^{Latch} are output propagation delay, t_{setup} and *FF* is setup time.

$$t_0 + t_{setup}\, f_p + t_{pcq}\text{-}ff + t_{Aext} < T_c + t_x + t_{Aint}^{Latch} \qquad (2)$$

There equation 2 is independent of timing circuit. The clock enabling signal is propagated from t setup – FF time window. As mentioned earlier $\sum x(D11)\times(t) = 0$ is sufficient clock. the *D11* can be evaluated and then *D11 (t+1) = D11 (t)*. There will be a question have large.

$$Pr[(D^{11}(t+1) = D^{11}(t) \Lambda (\sum x(D^{11} \times (t)=1)]$$

Thus LACG is power savor analyzed by worst-case toggling independence model from the theoretical approval where power saving is analyzed.

3. Methodology of Power Saving

The current mode signalling scheme perform current to voltage and obtain voltage mode clock signal current mode is integrated if it directly consumes CM signal in order to reduce power consumption. The clock gating can be implemented into the current model signaling shown in the Fig 6.

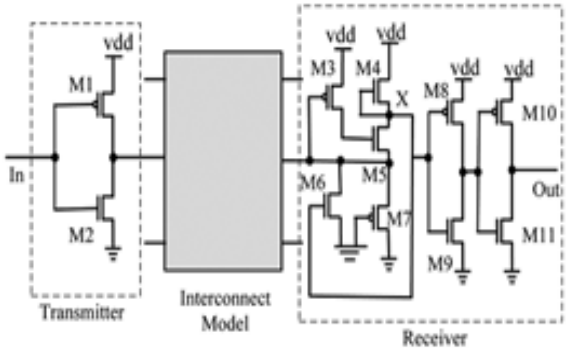

Figure 6. Previous CM schemes used an expensive transmpedance amp Rx which could in significant skew due to Vcm Shift if applied to CDNs

Current mode pulsed flip flop with Enable is the advance technology in current mode, CMPFFE perform well other than CM signaling. CMPFEF is similar to CM signal but here uses action low enable (EN) and if uses current-comparator. CC is a static storage call. A small signal analysis is expressed in CMPFFE.

$$Z_{in} = \frac{1}{gm1 + gm2} \qquad (3)$$

In CMPFFE, the transfer provides a push – pull current, and LACG is implemented in between CMPFFE. The transmitter receives voltage and clock signal that can be controlled by clock gating. Then, the current will distributed equally to all CMPFFE modes. In Figure 7, the transmitter circuit uses NAND – NOR design. Here, PMOS change from the supply then the NMOS will be in off state. Simultaneously NOR gate willies the negative clock, then NMOS will sink with current. While the M1 is off the PMOS get charged. Then Non- over login signal from the NAND – NOR will remove any short circuit current from transistor.

When the FF are toggled then

$$Pr\,[\sum_{Xcd11} x(t) = 0] = (1 - P)^k \qquad (4)$$

The Actual power obtained from the following analysis.

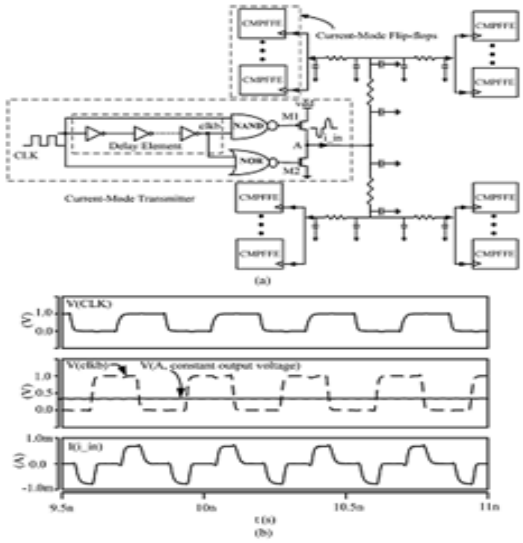

Figure 7. (a) The proposed CM Tx and CDN converts an VM input signal to a push – pull current with minimal interconnects voltage swing and distributes current equally to the CMPFFEs.
(b) Simulation waveforms confirm a VM input is converted to a constant CDN voltage and a represent push-pull current at each CMPFTE.

$$Pr = [\sum_{Xcd11} x(1) = 1 \Lambda x11\ (6 + 1) = 0] = [1-(1-p)^k](1-p) \quad (5)$$

In order to consulate LACG consider toggling as shown in the figure 3, the target of the *FF* will be

$$\{2(1-p)k - [1-(1-p)k]\}\ \frac{Cff + CLK}{3} - Pcx = [3(1-p)k-1]\ \frac{Cff + CLK}{3} - Pcx \quad (6)$$

Summing up all the above components, the following result will be obtained

$$[1-(1-p)^k]\ cff + C_{Aint} + C_{Aint} + [1 = (1-p)^k + Kp] \quad (7)$$

From 6 and 7 rearrangement gives

$$C^{Save}_{dyn} = (1-p)^k\ \ (cff + clk + cff + co) - p(cx + kco) - \frac{Cff + CLK}{3} + C_{Aint} + cff + C0] \quad (8)$$

C_{ff}	C_{CLK}	$C_{ff} + CL_K$	C_Y	C_o	C_{Aint}
25-7	31.5	35-9	2.9	3.1	1.7

Table 1. Typical capacitance in 20 *Nm* process Technology values in 10^{-15} f

4. Experiments For Minimizing Logic Gates

From the equation 8, C^{Save} are decreasing with the increase of P and K substitute $C^{save} = 0$ in eqn 8 dependency between *P* and *q* from the fig 8 and from the table (1), we take 20 nm process technology library. When the (k,p) points fall in the curved LACG will loose power the capacitance measured in 10^{-5}.

To develop logic sharing model to minimize the gating cost, OR logic increases the amount of redundant clock pulses.

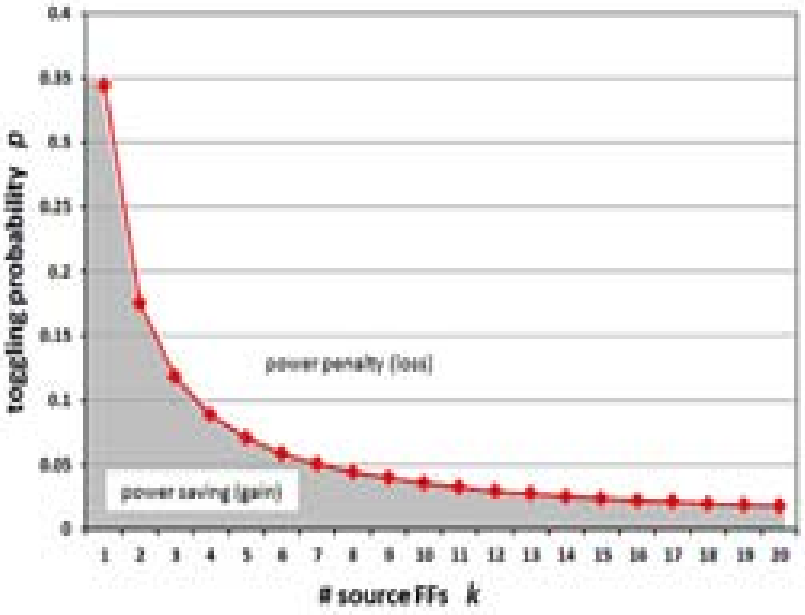

Figure 8. Power saving breakeven curve

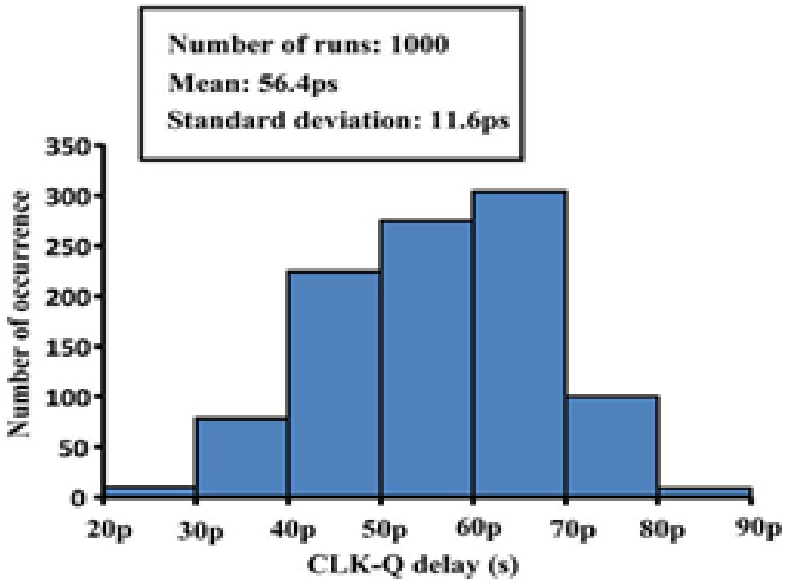

Figure 9. CLK – Q delay of Autogated clock gating

Since the clock is driven by Automating, the efficiency of the OR logic depends on best case and worst case. In CMPFFE, input transition is 50% and output transition is 50%. The CMPFFE have lower clock – *Q* delay. The Monto carcoa simulation of *clk* – *Q* delay of Autogated clock gating is shown in figure 9. The flip-flop power will not represent the overall power consumption of the current mode. Power saving can be shown in CMPFFE with total power and the additional static power.

Fre. (GHz)	# of sinks	CE[1] (mm)	Total CDN power (mW)		Total power consumption including FFs and CDNs (mW)					% Saving compared to			
			VM CDN	CM CDN	MS DFF sys.	Tra. PFF sys.	CPEFF sys.	DDPFF sys.	CMPFFE sys.[2]	MS DFF sys.	Tra. PFF sys.	CPEFF sys.	DDPFF sys.
2	4	0.48	0.72	0.26	0.92	1.03	0.96	0.97	0.83	9.82	19.63	13.95	14.66
	16	0.96	3.03	0.54	3.81	4.26	3.99	4.02	2.79	26.8	34.49	30.03	30.58
	64	1.92	10.62	1.13	13.75	15.54	14.46	14.58	10.16	26.14	34.66	29.74	30.36
	256	3.84	44.28	4.52	56.82	63.99	59.64	60.15	40.62	28.52	36.53	31.9	32.48
	1024	7.69	184.90	18.25	235.07	263.74	246.34	248.38	162.63	30.81	38.34	33.98	34.52
3	4	0.48	1.07	0.30	1.36	1.48	1.43	1.45	0.90	33.89	39.23	36.85	37.89
	16	0.96	4.23	0.58	5.40	5.88	5.66	5.76	3.00	44.42	48.96	46.94	47.82
	64	1.92	15.56	1.15	20.23	22.15	21.26	21.64	10.72	47.00	51.59	49.55	50.45
	256	3.84	66.51	4.91	85.19	92.88	89.29	90.83	43.64	48.77	53.01	51.12	51.95
	1024	7.69	270.02	19.78	344.77	375.49	361.16	367.30	174.71	49.33	53.47	51.62	52.43
4	4	0.48	1.13	0.33	1.52	1.68	1.60	1.62	1.00	34.26	40.37	37.38	38.3
	16	0.96	4.24	1.04	5.81	6.43	6.11	6.21	3.73	35.81	42.04	39.00	39.95
	64	1.92	21.88	1.20	28.15	30.65	29.37	29.75	11.94	57.58	61.03	59.34	59.86
	256	3.84	89.38	5.29	114.47	124.45	119.33	120.87	48.30	57.81	61.19	59.63	60.04
	1024	7.69	361.37	20.03	461.72	501.66	481.18	487.32	192.06	58.40	61.71	60.09	60.59
5	4	0.48	1.70	0.34	2.19	2.38	2.30	2.32	1.06	51.46	55.45	53.75	54.22
	16	0.96	7.18	1.38	9.13	9.92	9.56	9.66	4.31	52.83	56.56	54.96	55.40
	64	1.92	27.34	1.62	34.95	38.08	36.68	37.06	13.33	61.85	64.99	63.65	64.03
	256	3.84	112.05	5.78	143.28	155.83	150.19	151.73	52.65	63.26	66.21	64.95	65.30
	1024	7.69	453.62	20.37	578.55	628.72	606.20	612.34	207.76	64.09	66.95	65.73	66.07

Table 2. Power Saving Description

The maximum cost perfect matching (MCPM) algorithm used to satisfy *wcc(i) = 0* then the gating logic of *ffi* and *ffj* are not merged. A heuristic solution was proposed by LACG successfully.

5. Experimentation Results

The LACG is implemental with CMPFFE and power can be saved in control blocks with register file dynamic power is 80% and static power is 20%. The gating technology represented in Figure 3 is verified by EDA tool and the original circuit was introduced. Clock gating technology employed by the design LACG is a gate-level gating technology. Then power can be reduce power saving which is explained in the following figure 10.

In figure 10 clock, c_{dyn} is 4770 of which 1060 pf has been reduced by LACG total dynamic power reduction where 22% power saving is achieved only by LACG. The dynamic power depends on logic and static power independent of switching activity. The Static power is 21% of total power taking all factors into account 22% of clock c_{dyn} reductions were translated into 12.5% reduction of total power.

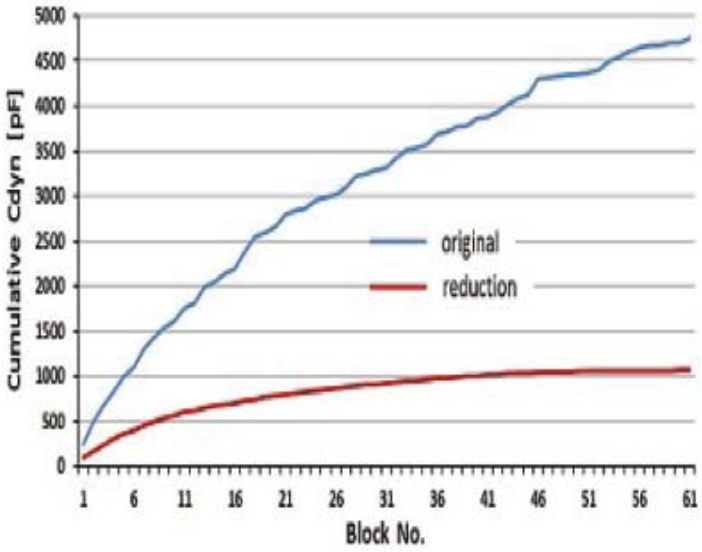

Figure 10. Cumulative *cdyn b*efore gating and the amount of reduction achieved by LACG

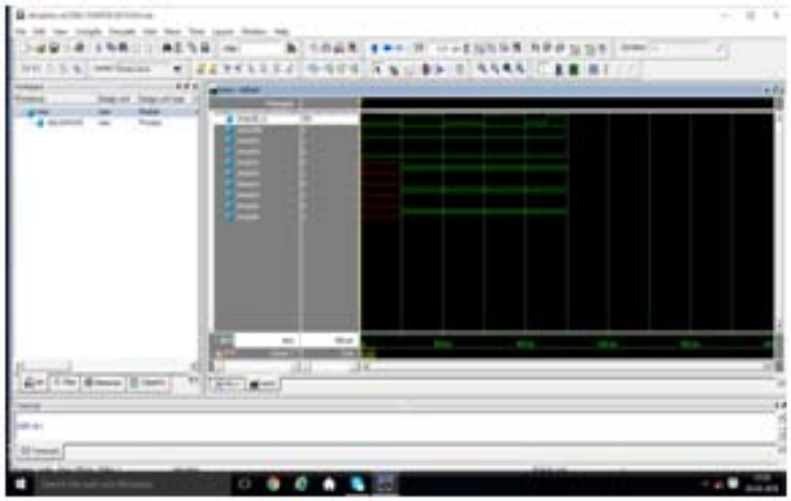

Figure 11. Simulation of clock gating

6. Conclusion

Look ahead clock gating explained in this work is very helpful for reducing Clock switching power. Clock signal avoids timing constraints from existing clock gating technology closed model of the power saving technique by Auto gated Flip flop that is implemented in gating logic. The gating logic will optimize the *FF* for Joint gating. While this paper discussed the power saving when global clock is given into the logic gates costuming of *ff* by group and yield high power saving and this matter is left for further research.

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